RELIABILITY REPORT

FOR

MAX7310AxE

PLASTIC ENCAPSULATED DEVICES

July 25, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX7310 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX7310 provides 8-bit parallel input/output port expansion for SMBus™-compatible and I^2C-compatible applications. The MAX7310 consists of an input port register, an output port register, a polarity inversion register, a configuration register, a bus timeout register, and an SMBus/I^2C-compatible serial interface. The system master can invert the MAX7310 input data by writing to the active-high polarity inversion register. The system master can enable or disable bus timeout by writing to the bus timeout register.

Any of the eight I/O ports can be configured as input or output. An active-low reset input sets the eight I/Os as inputs. Three address-select pins configure one of 56 slave ID addresses.

The MAX7310 is available in 16-pin thin QFN, TSSOP, and QSOP packages and is specified over the -40°C to +125°C automotive temperature range.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +6V
I/O1–I/O7 as an Input	(VSS - 0.3V) to (VDD + 0.3V)
I/O0 as an Input	(VSS - 0.3V) to +6V
SCL, SDA, AD0, AD1, AD2, RESET	(VSS - 0.3V) to +6V
DC Current on I/O0	+400µA
DC Current on I/O1 to I/O7	±50mA
Maximum GND and V+ Current	180mA
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin TSSOP	457mW
16-Pin QSOP	667mW
16-Pin Thin QFN	1349mW
Derates above +70°C	
16-Pin TSSOP	5.7mW/°C
16-Pin QSOP	8.3mW/°C
16-Pin Thin QFN	16.9mW/°C

II. Manufacturing Information

A. Description/Function:	2-Wire-Interfaced 8-Bit I/O Port Expander with Reset
B. Process:	S6 (0.6 micron CMOS)
C. Number of Device Transistors:	10,256
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia, Thailand, Korea, Hong Kong or Philippines
F. Date of Initial Production:	January, 2003

III. Packaging Information

A. Package Type:	**16 Lead TSSOP**	**16-Lead QSOP**	**16-Lead QFN (3x3)**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0030	# 05-9000-0031	# 05-9000-0111
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	70 x 78 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si (Aluminum/ Silicon)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 24.13 \times 10^{-9}$ $\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec #06-6040) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The DW52 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX7310AxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP QSOP QFN	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

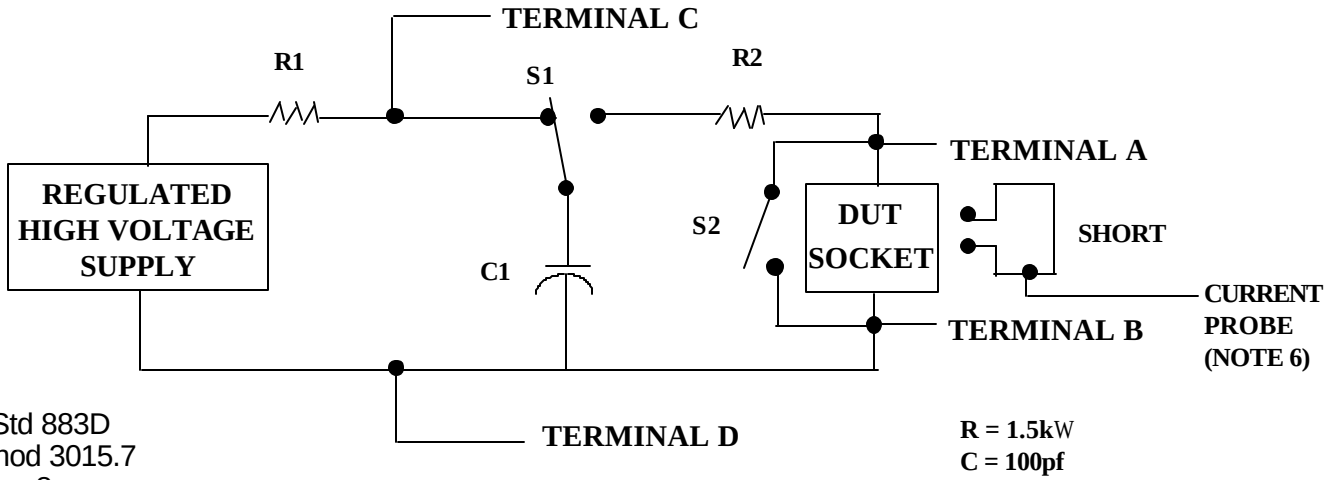
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

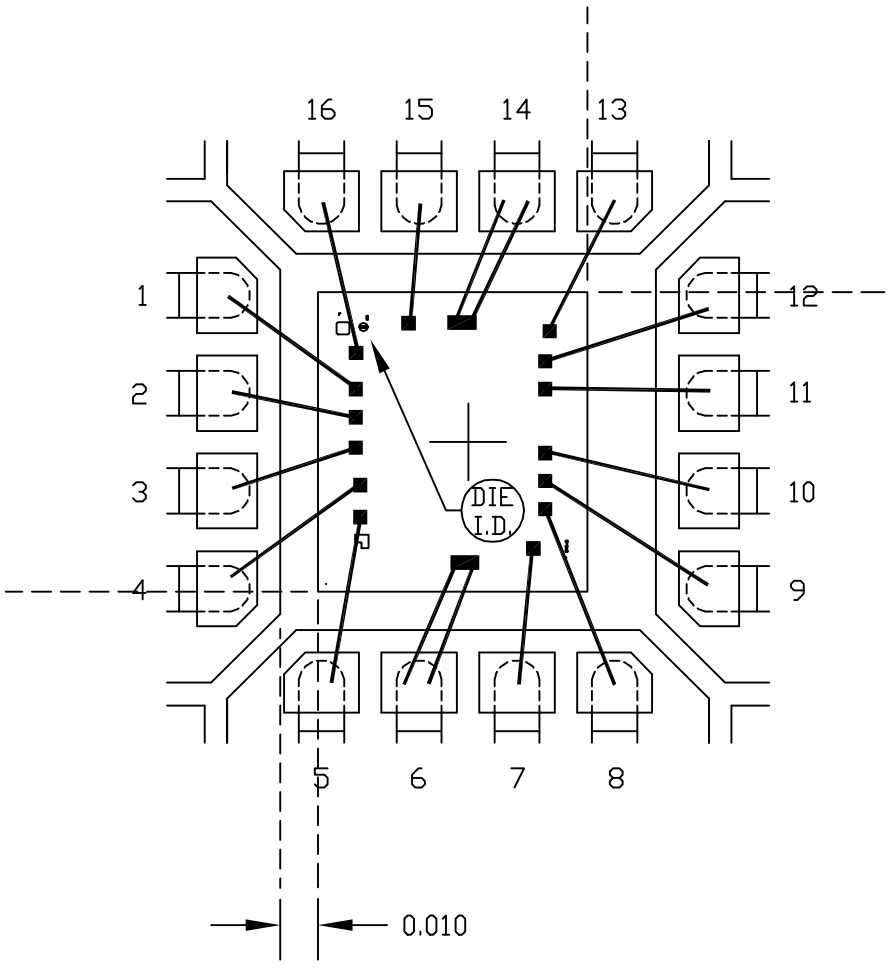
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

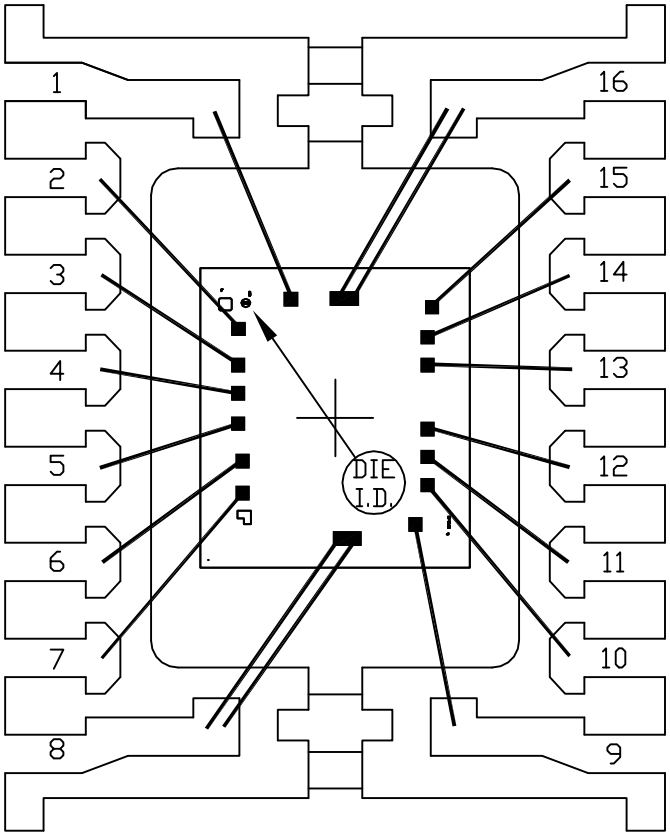


Mil Std 883D
Method 3015.7
Notice 8

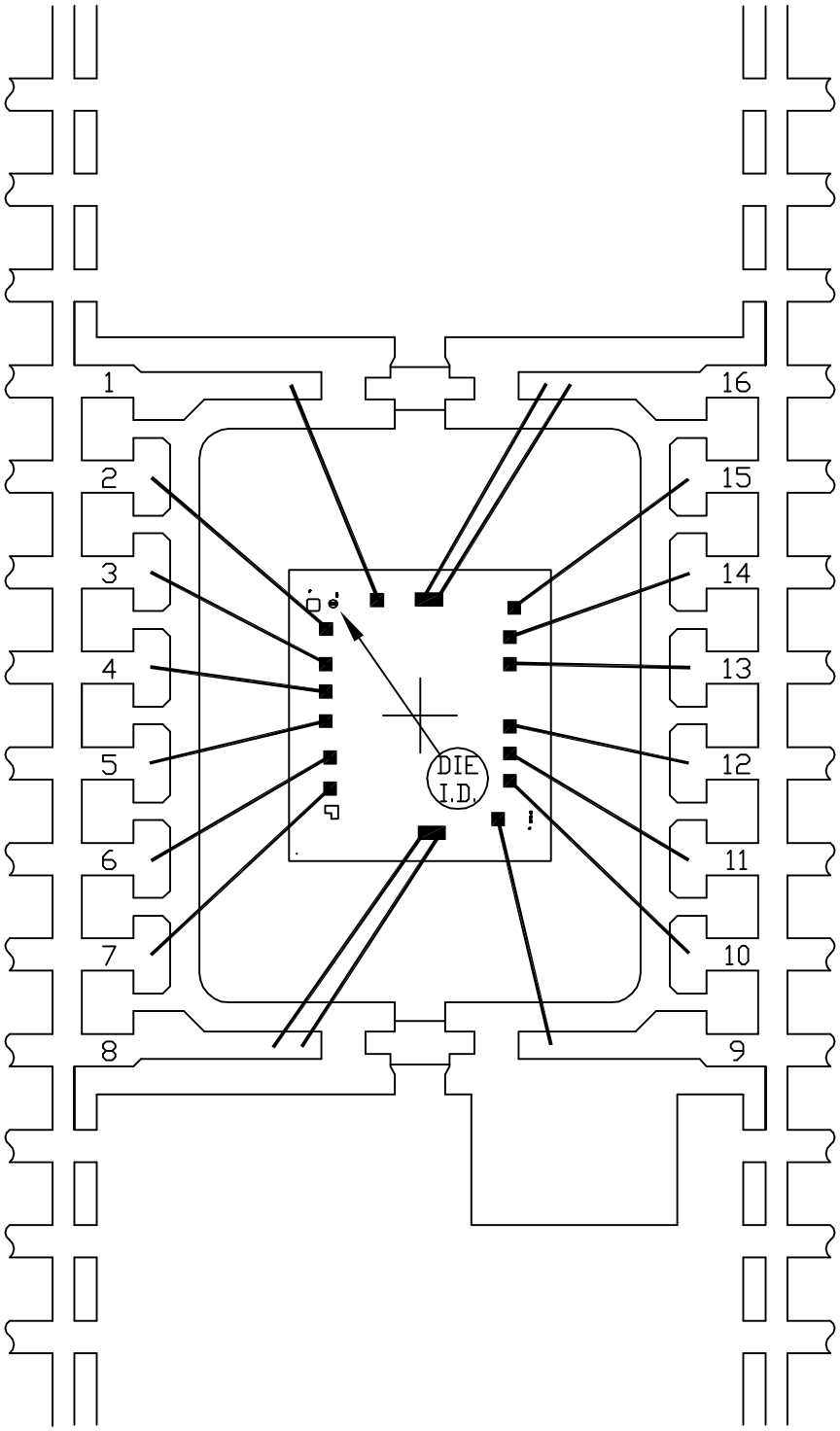
4x4x0.80mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T1644-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0111	REV: A
	DESIGN				



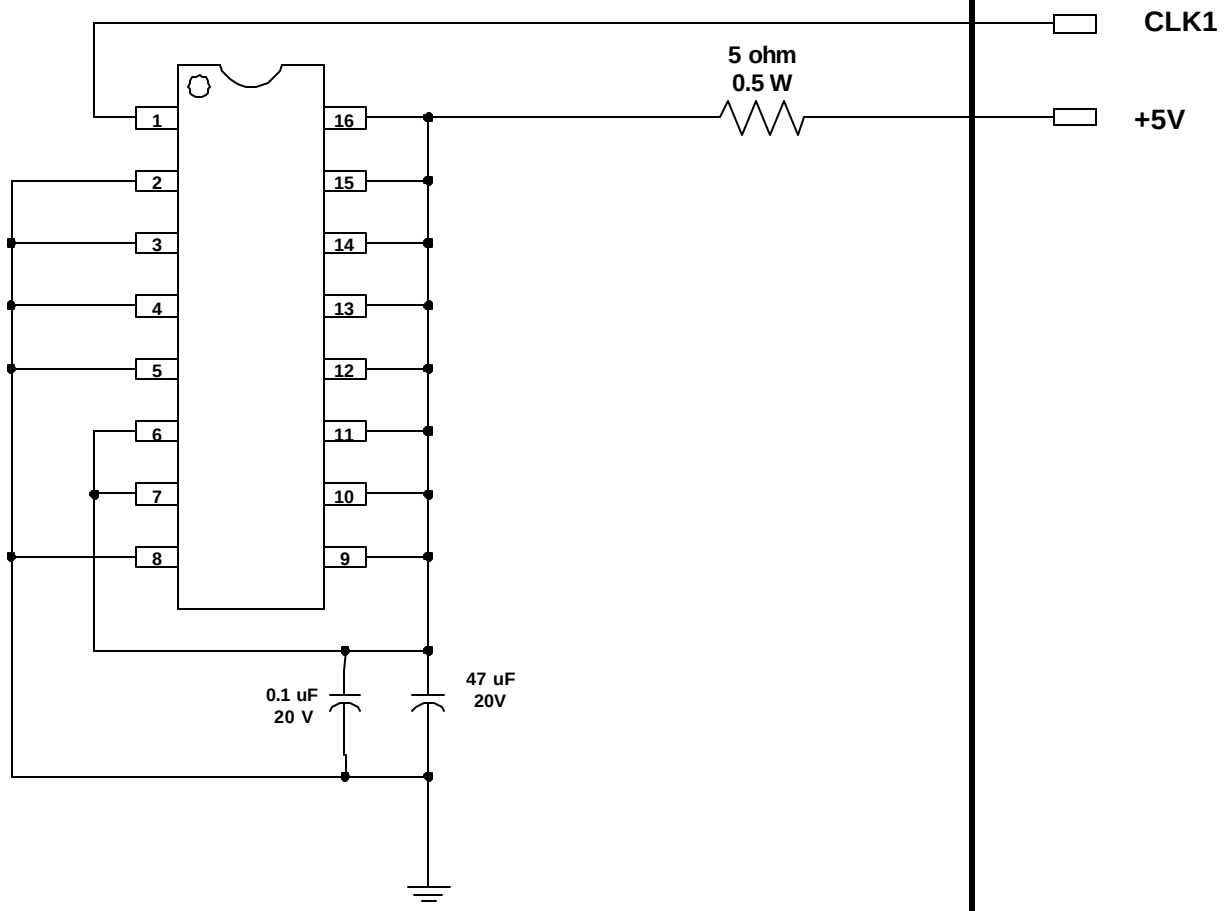
PKG. CODE: E16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X130	PKG.			BOND DIAGRAM #: 05-9000-0031	REV: A
	DESIGN				



PKG. CODE: U16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 118X154	PKG.			BOND DIAGRAM #: 05-9000-0030 / REV: A
	DESIGN			

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 7310
PACKAGE: 16-TSSOP
MAX. EXPECTED CURRENT = 15 mA

DRAWN BY: TODD BEJSOVEC 4/25/02
NOTES: CLK1 = 0-5 VOLTS, 200 KHz.
USE JARVIS OVEN CLOCK PROGRAM #30.