

RELIABILITY REPORT  
FOR  
**MAX3670EGJ**  
PLASTIC ENCAPSULATED DEVICES

April 2, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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## Conclusion

The MAX3670 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX3670 is a low-jitter 155MHz/622MHz reference clock generator IC designed for system clock distribution and frequency synchronization in OC-48 and OC-192 SONET/SDH and WDM transmission systems. The MAX3670 integrates a phase/frequency detector, an operational amplifier (op amp), prescaler dividers and input/output buffers. Using an external VCO, the MAX3670 can be configured easily as a phase-lock loop with bandwidth programmable from 15Hz to 20kHz.

The MAX3670 operates from a single +3.3V or +5.0V supply, and dissipates 150mW (typ) at 3.3V. The operating temperature range is from -40°C to +85°C. The chip is available in a 5mm 5 5mm, 32-pin QFN package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage	-0.5V to +7.0V
Voltage at C2+, C2-, THADJ, CTH, GSEL1,GSEL2,GSEL3, /LOL,RSEL,REFCLK-,REFCLK+,VSEL,VCOIN+,VCOIN-, VC,POLAR,PSEL1,PSEL2,COMP,OPAMP+,OPAMP- PECL Output Current (MOUT+,MOUT-,POUT+,POUT-)	-0.5V to (V <sub>CC</sub> + 0.5V) 56mA
Storage Temp.	-65°C to +160°C
Operating Temp.	-40°C to +85°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
32-Pin QFN-EP	1.70W
Derates above +70°C	
32-Pin QFN-EP	21.3mW/°C

## II. Manufacturing Information

A. Description/Function:	Low Jitter 155MHz/622MHz Clock Generator
B. Process:	GST2 (High-Speed Double Poly-Silicon Bipolar Process)
C. Number of Device Transistors:	2478
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	September, 2001

## III. Packaging Information

A. Package Type:	<b>32-Lead QFN</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-7001-0548
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	80 x 76 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.4 microns (as drawn)
F. Minimum Metal Spacing:	1.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

### A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 10.78 \times 10^{-9} \quad \lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (#06-7024) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The HT17 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX3670EGJ**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)				
	Ta = 150°C Biased Time = 192 hrs. Junction Temperature = 150°C	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

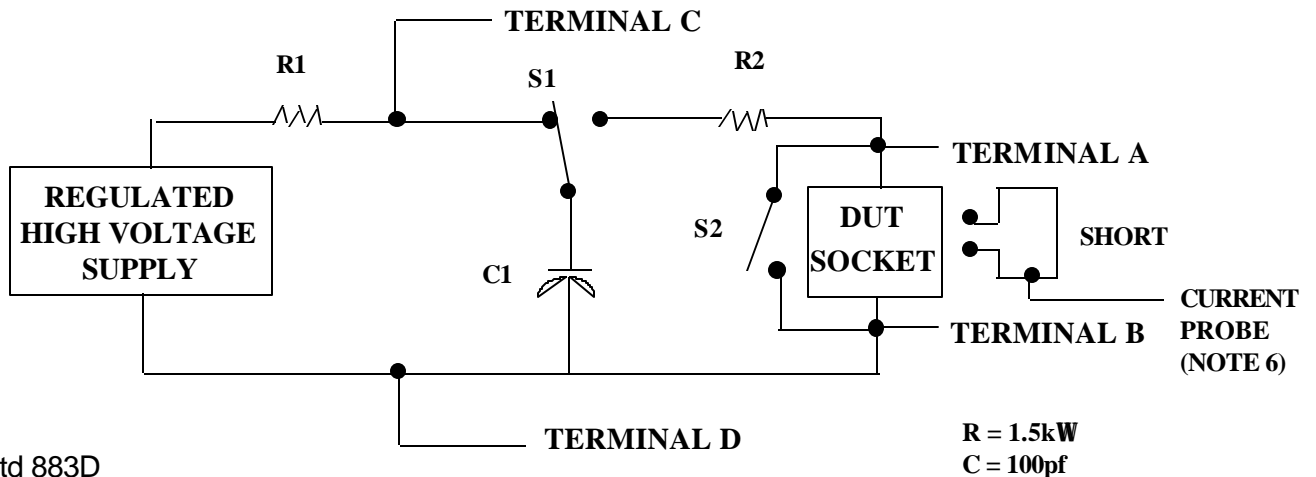
2/ No connects are not to be tested.

3/ Repeat pin combination 1 for each named Power supply and for ground

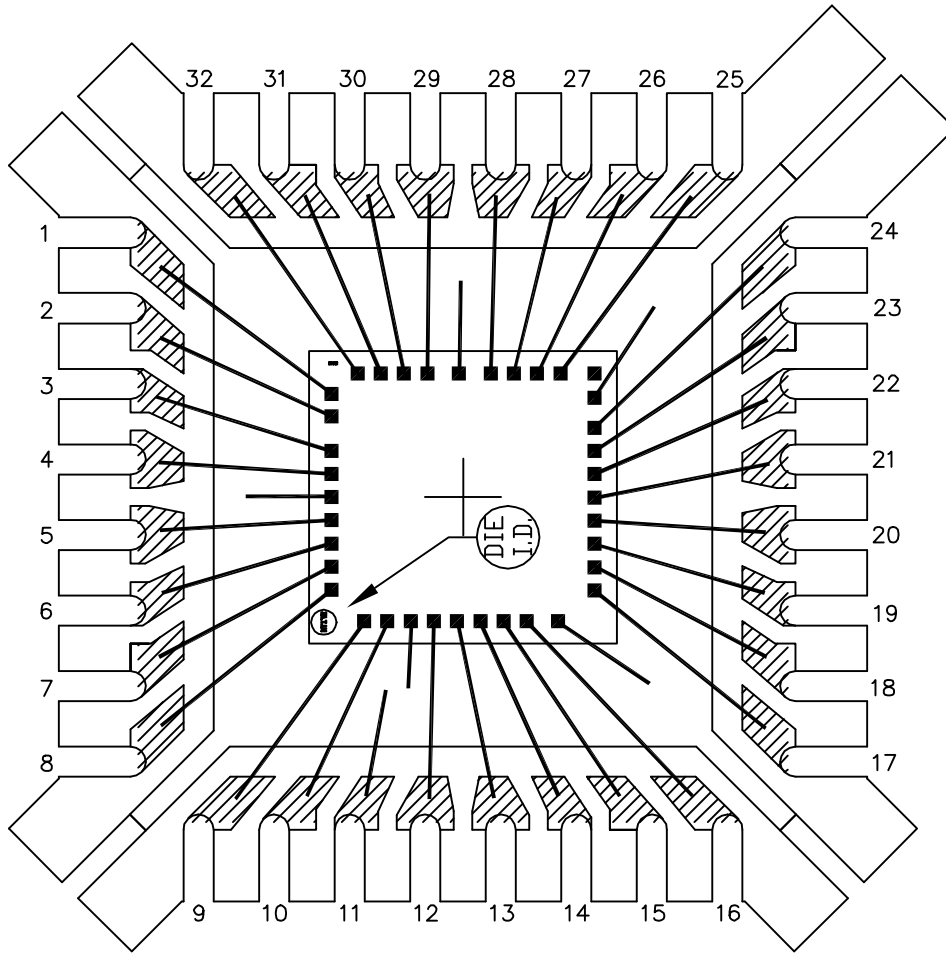
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



EXPOSED PAD PKG.



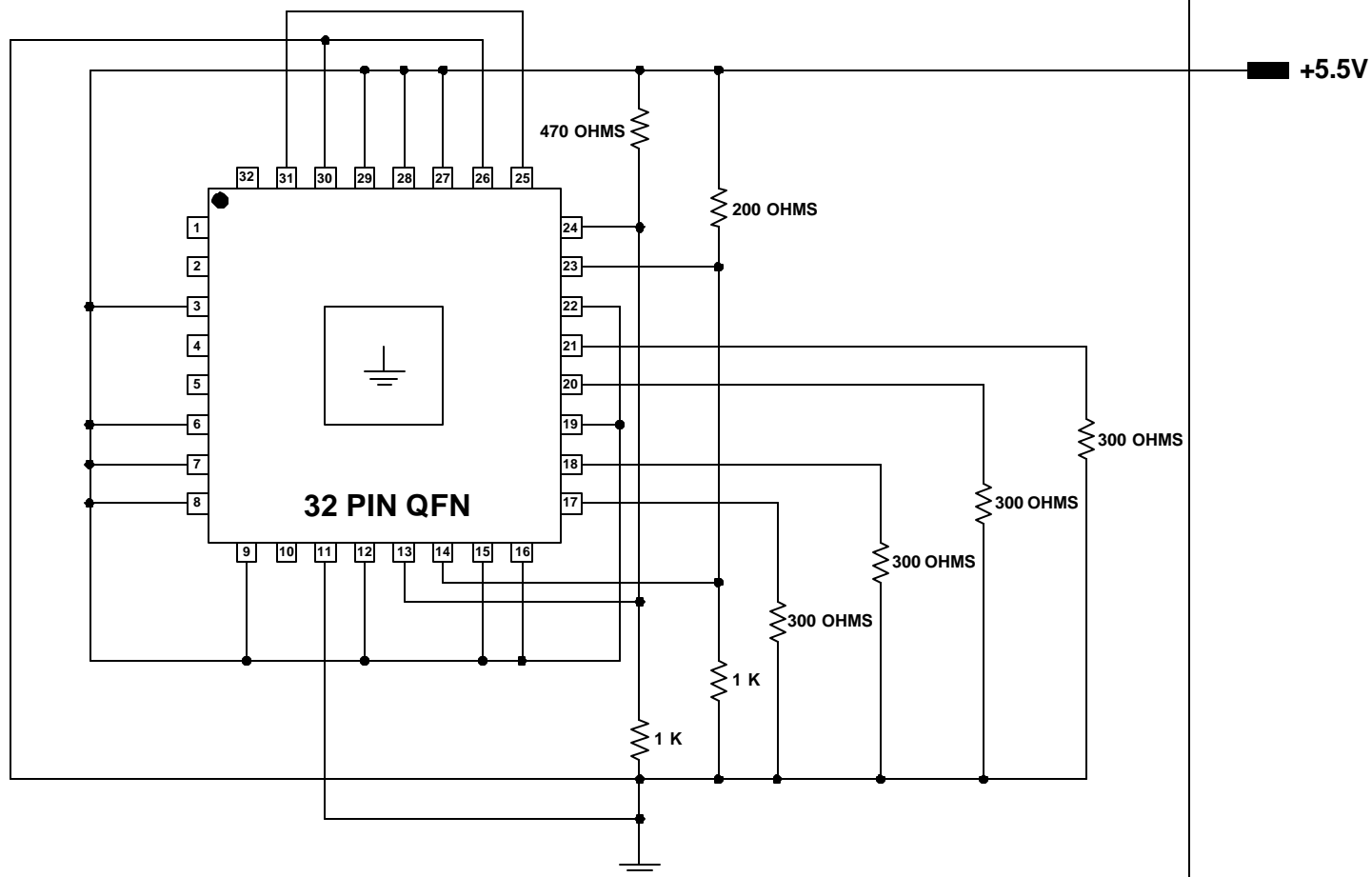
 BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G3255-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG. DESIGN		4/24/01 4/24/01	BOND DIAGRAM #: 05-7001-0548	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 3670

DRAWN BY: TEK TAN

MAX. EXPECTED CURRENT = 121 mA

NOTES: Connect Exposed Paddle To GROUND.  
Temp. = 85c