

RELIABILITY REPORT  
FOR  
**MAX3232xxE**  
PLASTIC ENCAPSULATED DEVICES

May 6, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord  
Quality Assurance  
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl  
Quality Assurance  
Executive Director

## Conclusion

The MAX3232 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX3232 transceiver has a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. This device requires only four small 0.1 $\mu$ F external charge-pump capacitors. The MAX3232 is guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels.

This device has 2 receivers and 2 drivers. The MAX3232 is pin, package, and functionally compatible with the industry-standard MAX232.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V <sub>CC</sub>	-0.3V to +6V
V <sub>+</sub> (Note 1)	-0.3V to +7V
V <sub>-</sub> (Note 1)	+0.3V to -7V
V <sub>+</sub> + V <sub>-</sub> (Note 1)	+13V
Input Voltages	
T <sub>IN</sub> , /SHDN, /EN	-0.3V to +6V
MBAUD	-0.3V to (V <sub>CC</sub> + 0.3V)
R <sub>IN</sub>	$\pm$ 25V
Output Voltages	
T <sub>OUT</sub>	$\pm$ 13.2V
R <sub>OUT</sub>	-0.3V to (V <sub>CC</sub> + 0.3V)
Short-Circuit Duration	
T <sub>OUT</sub>	Continuous
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
16-Pin DIP	842mW
16-Pin NSO	696mW
16-Pin WSO	762mW
16-Pin TSSOP	533mW
Derates above +70°C	
16-Pin DIP	10.53mW/°C
16-Pin NSO	8.70mW/°C
16-Pin WSO	9.52mW/°C
16-Pin TSSOP	6.70mW/°C

**Note 1:** V<sub>+</sub> and V<sub>-</sub> can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

## II. Manufacturing Information

- A. Description/Function: 3.0V to 5.5V, Low-Power, up to 1Mbps, True RS-232 Transceiver  
Using Four 0.1 $\mu$ F External Capacitors
- B. Process: S3 (Standard 3 micron silicon gate CMOS)
- C. Number of Device Transistors: 339
- D. Fabrication Location: California or Oregon, USA
- E. Assembly Location: Philippines, Malaysia, Korea, or Thailand
- F. Date of Initial Production: October, 1994

## III. Packaging Information

- | A. Package Type:  | 16-Pin PDIP                  | 16-Pin WSO               | 16-Pin NSO               | 16-Pin TSSOP           |
|---|------------------------------|--------------------------|--------------------------|------------------------|
| B. Lead Frame:  | Copper                       | Copper                   | Copper                   | Copper                 |
| C. Lead Finish:   | Solder Plate                 | Solder Plate             | Solder Plate             | Solder Plate           |
| D. Die Attach:  | Silver-filled Epoxy          | Silver-filled Epoxy      | Silver-filled Epoxy      | Silver-filled Epoxy    |
| E. Bondwire:  | Gold (1.3 mil dia.)          | Gold (1.3 mil dia.)      | Gold (1.3 mil dia.)      | Gold (1.3 mil dia.)    |
| F. Mold Material:   | Epoxy with silica filler     | Epoxy with silica filler | Epoxy with silica filler | Epoxy w/ silica filler |
| G. Assembly Diagram:  | # 05-1901-0246               | # 05-1901-0255           | # 05-1901-0249           | # 05-1901-0262         |
| H. Flammability Rating:   | Class UL94-V0                | Class UL94-V0            | Class UL94-V0            | Class UL94-V0          |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 (all package styles) |                          |                          |                        |

## IV. Die Information

- A. Dimensions: 123 x 87 mils
- B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO<sub>2</sub>
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

### A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 520 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 2.09 \times 10^{-9} \quad \lambda = 2.09 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5054) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The RS21-2 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
**Reliability Evaluation Test Results**

**MAX3223xxE**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>PACKAGE</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test (Note 1)</b>					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		520	0
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP	77	0
			NSO	77	0
			TSSOP	77	0
			WSO	77	2
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

2/ No connects are not to be tested.

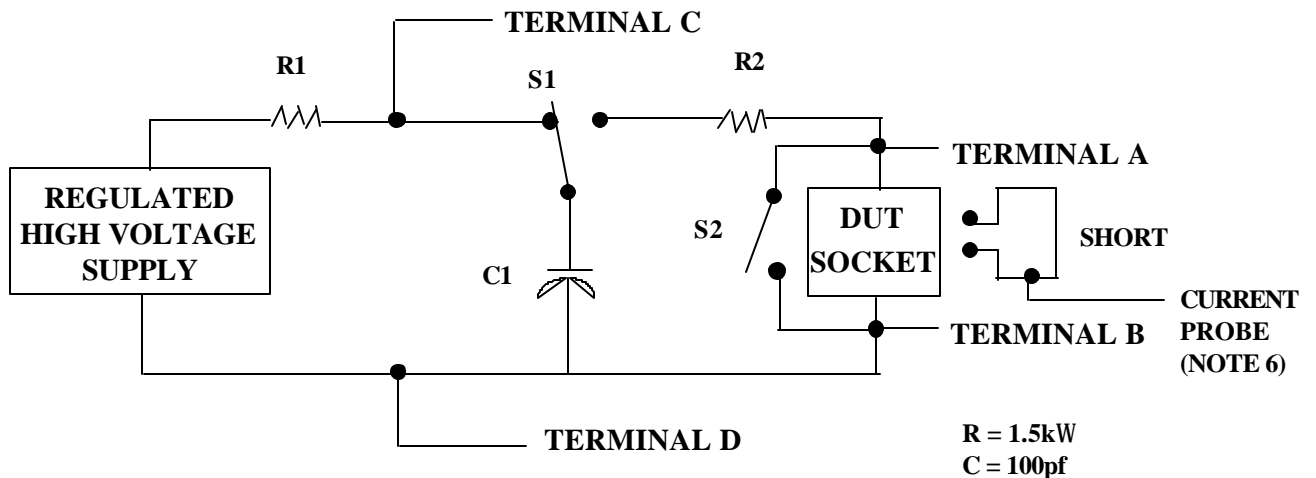
3/ Repeat pin combination I for each named Power supply and for ground

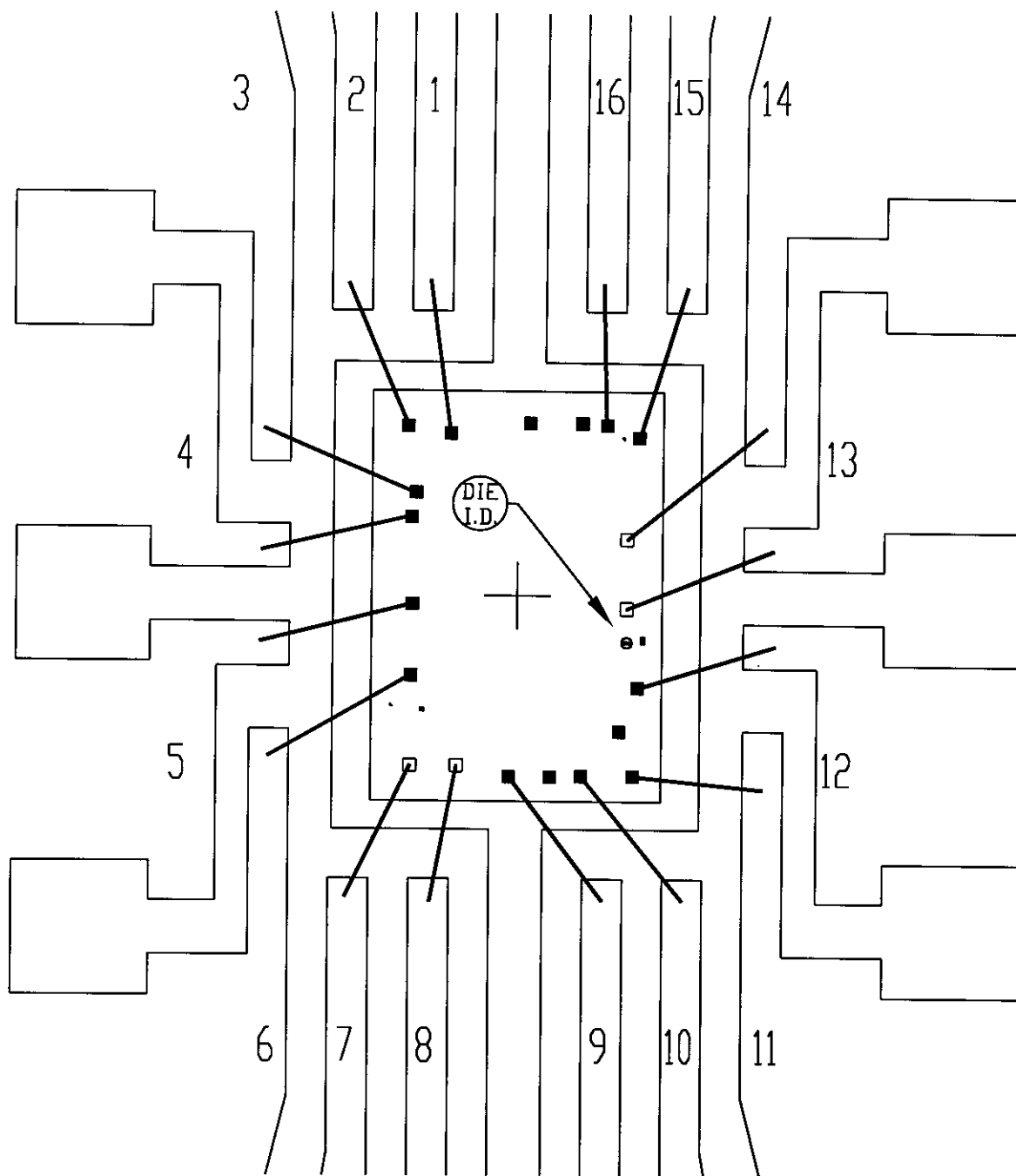
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: P16-1

CAV./PAD SIZE:  
110x140

PKG.  
DESIGN

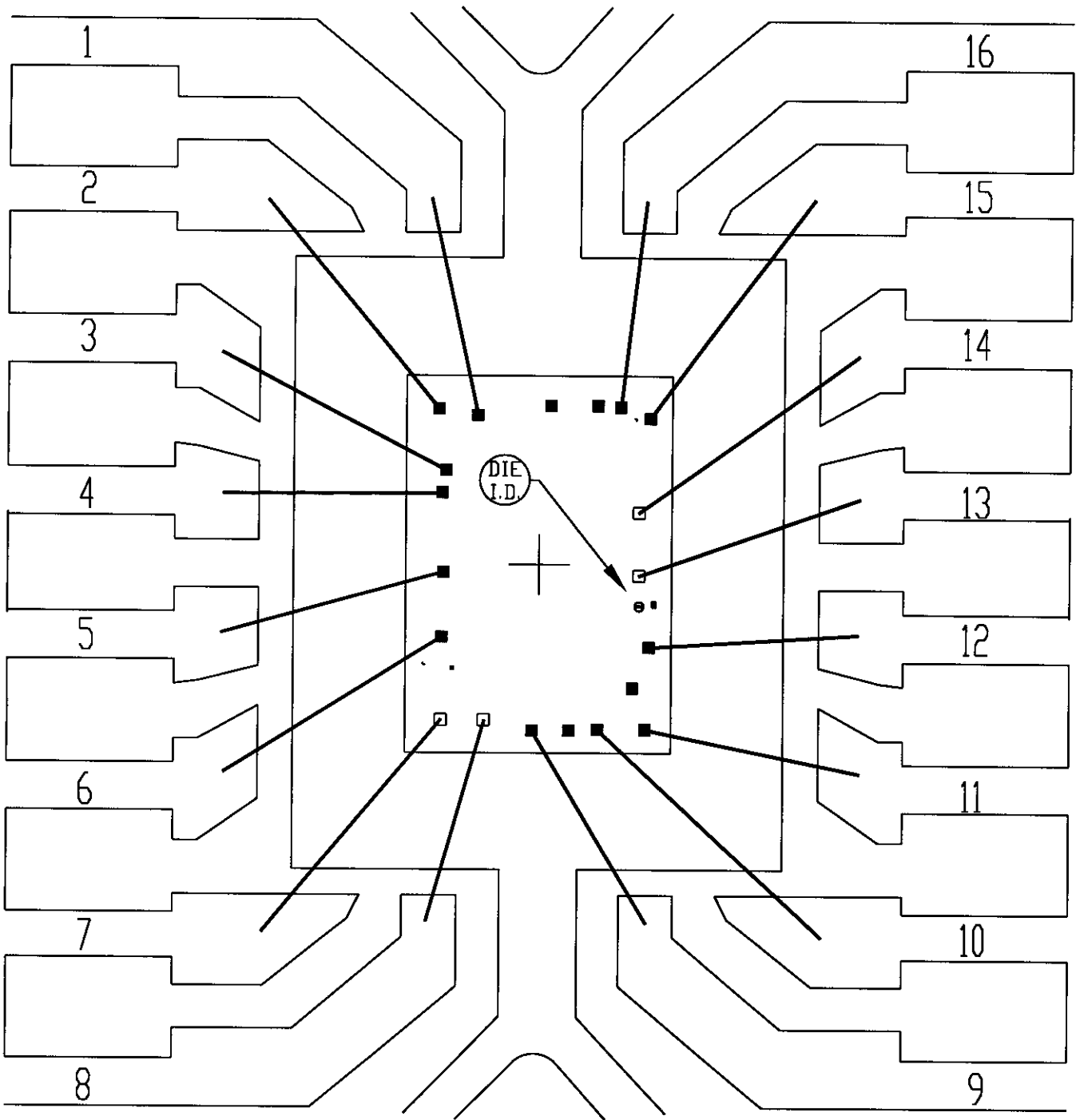
SIGNATURES

DATE

**MAXIM**  
CONFIDENTIAL & PROPRIETARY

BOND DIAGRAM #:  
05-1901-0246

REV:  
A



PKG. CODE: W16-3

CAV./PAD SIZE: 160 X 200

PKG.  
DESIGN

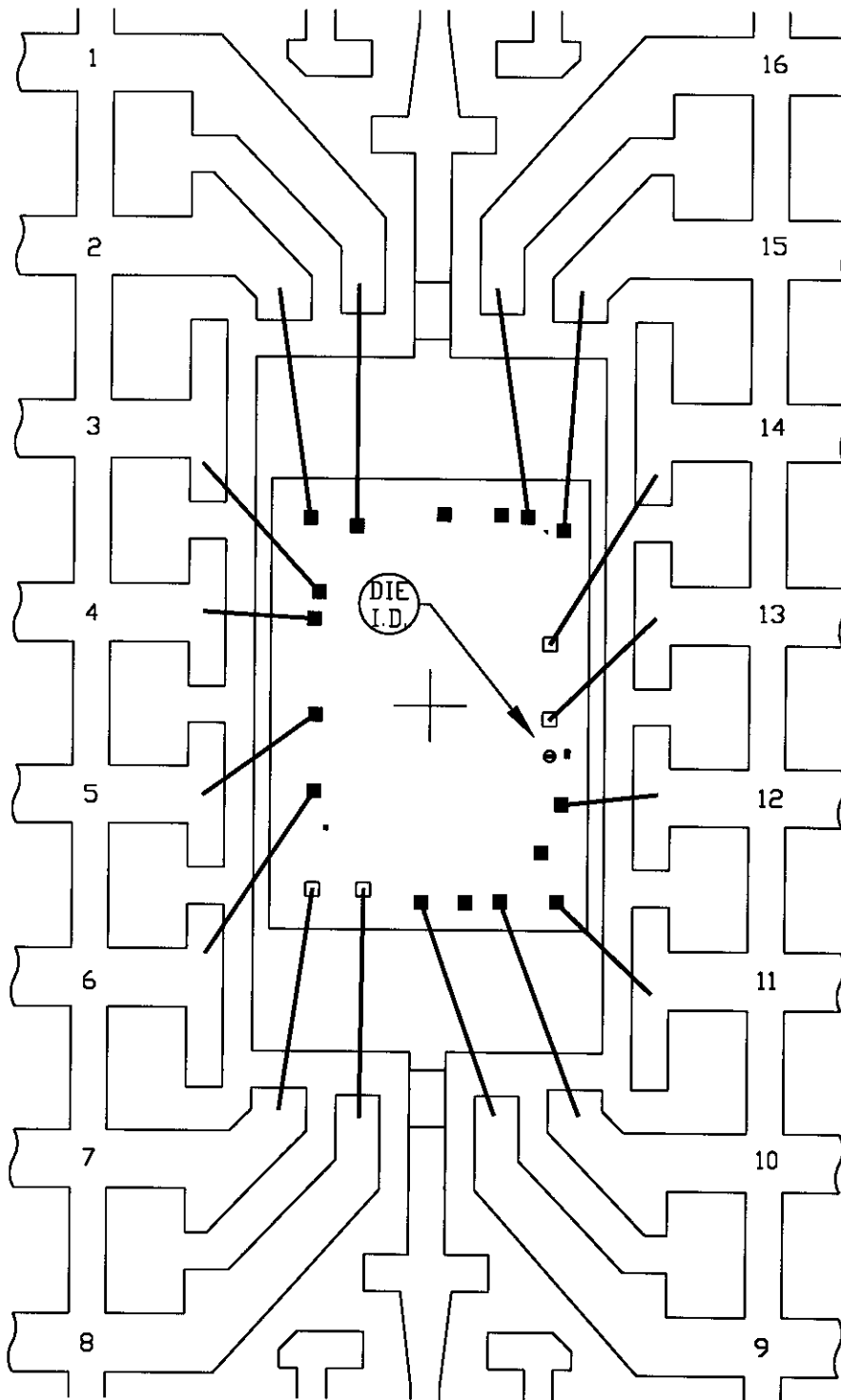
SIGNATURES

DATE

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BOND DIAGRAM #:  
05-1901-0255

REV:  
A



PKG. CODE: S16-5

CAV./PAD SIZE: 96X190

SIGNATURES

DATE

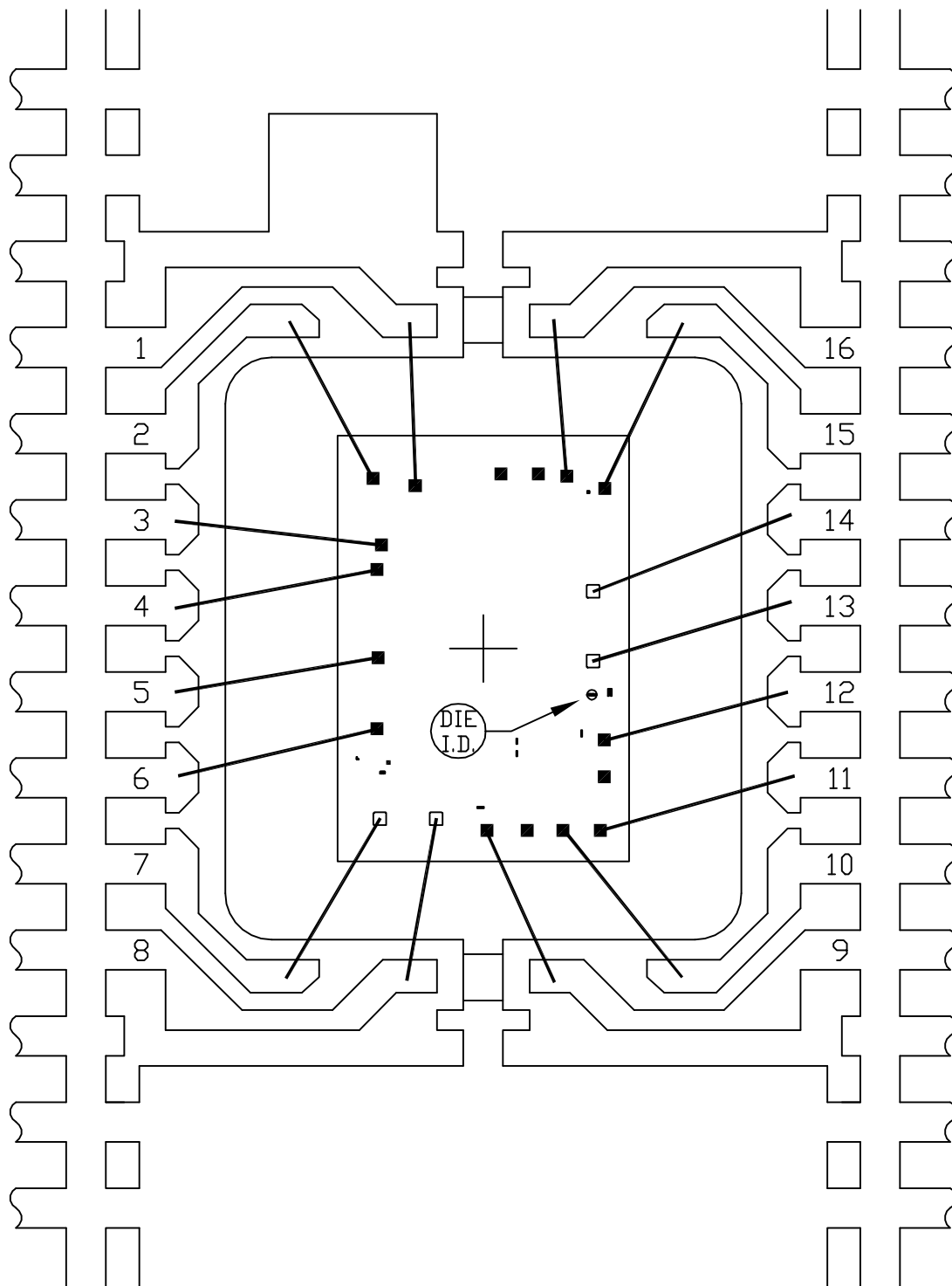
**MAXIM**  
CONFIDENTIAL & PROPRIETARY

PKG.  
DESIGN

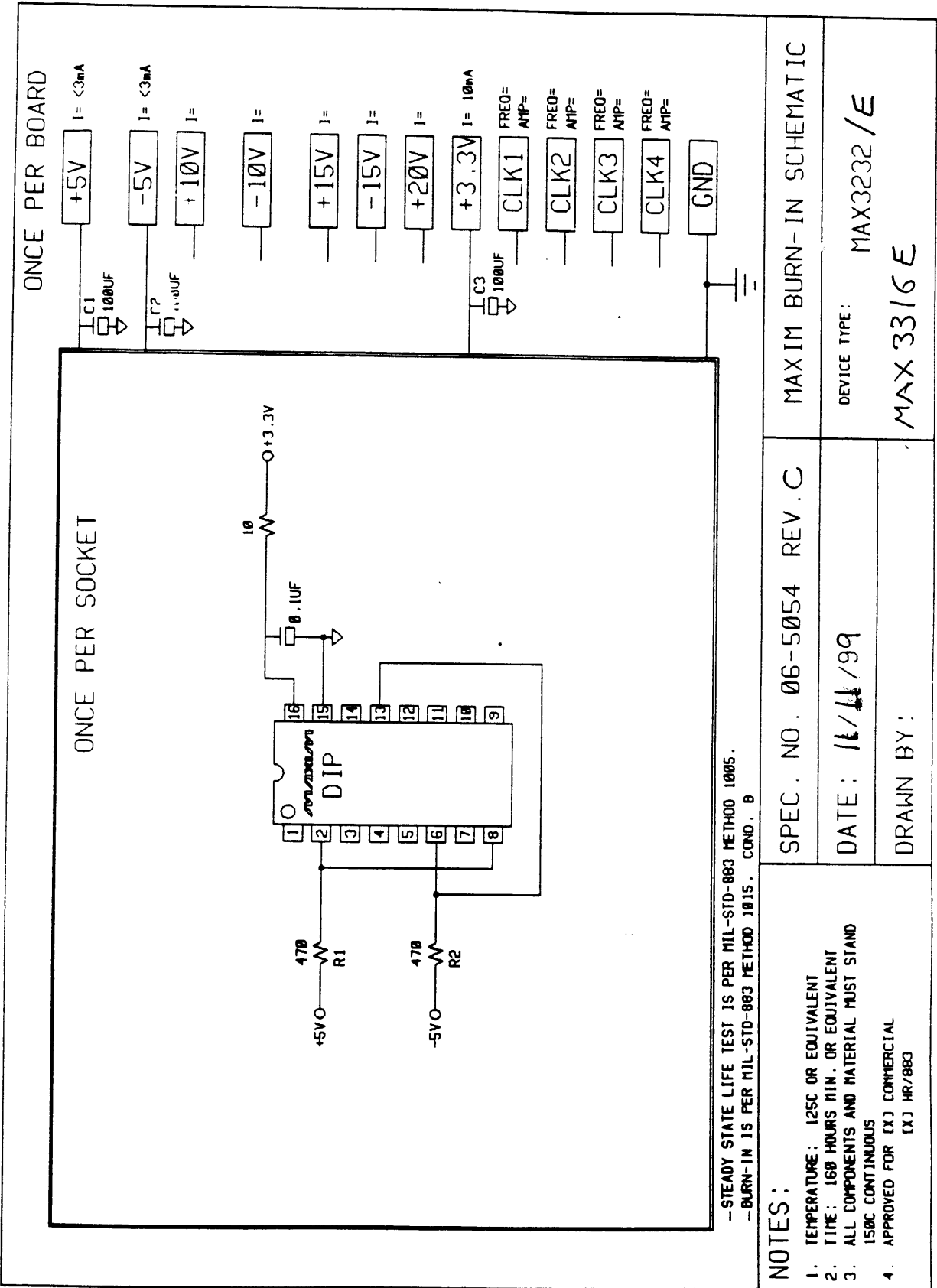
8/21/00  
8-22-00

BOND DIAGRAM #:  
05-1901-0249

REV:  
A



PKG. CODE: A16-2		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 154X173	PKG. DESIGN			BOND DIAGRAM #: 05-1901-0262	REV: A



-STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.  
 -BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL (X) HR/88G

SPEC. NO. 06-5054 REV. C

DATE: 11/11/99

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE: MAX3232/E  
 MAX 3316E