

RELIABILITY REPORT
FOR
MAX1697TEUT
PLASTIC ENCAPSULATED DEVICES

September 10, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX1697T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1697T ultra-small, monolithic, CMOS charge-pump voltage inverter accepts an input voltage ranging from +1.25V to +5.5V. This device features an ultra-low 12 output resistance, permitting loads of up to 60mA with maximum efficiency. The MAX1697T has an operating frequencies of 125kHz, or 250kHz. Its small external components and micropower shutdown mode make this device ideal for both battery-powered and board-level voltage conversion applications.

Oscillator control circuitry and four power MOSFET switches are included on-chip. Applications include generating a negative supply from a +5V or +3.3V logic supply to power analog circuitry. All versions come in a 6-pin SOT23 package and deliver 60mA.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN to GND	-0.3V to +6V
C1+, SHDN to GND	-0.3V to (VIN + 0.3V)
C1- to GND	(VOUT - 0.3V) to + 0.3V
OUT to GND	+0.3V to -6V
OUT Output Current	90mA
OUT Short-Circuit to GND	Indefinite
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
6-Pin SOT (Note 1)	1.1mW
Derate above +70°C	
6-Pin SOT (Note 1)	14mW/°C

Note 1: Thermal properties are specified with product mounted on the PC board with one square-inch of copper area and still air.

II. Manufacturing Information

- A. Description/Function: 60mA, SOT23 Inverting Charge Pump with Shutdown
- B. Process: S3 (Standard 3 micron silicon gate CMOS)
- C. Number of Device Transistors: 275
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Malaysia or Thailand
- F. Date of Initial Production: February, 1997

III. Packaging Information

- A. Package Type: **6-Lead SOT Flip-Chip**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: N/A
- E. Bondwire: 6 Mil Dia Ball
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-2301-0011
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

- A. Dimensions: 90 x 45 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 134 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 8.10 \times 10^{-9}$$

$$\lambda = 8.10 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80-piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5436) shows the static Burn-In circuit. Maxim also performs quarterly 1000-hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PY22-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
 Reliability Evaluation Test Results
MAX1697TEUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		134	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SOT23	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

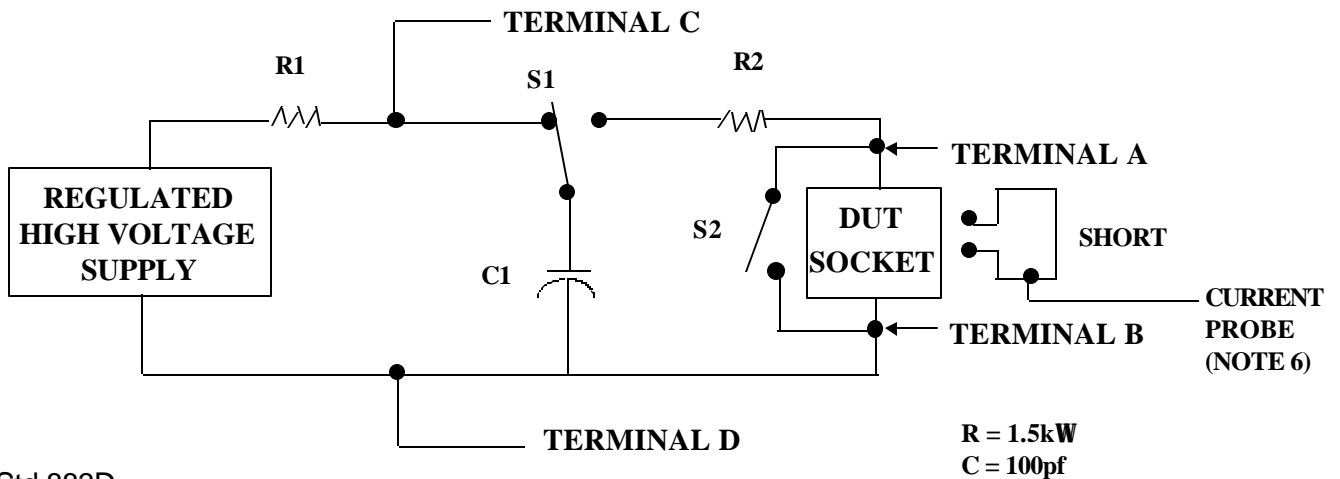
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

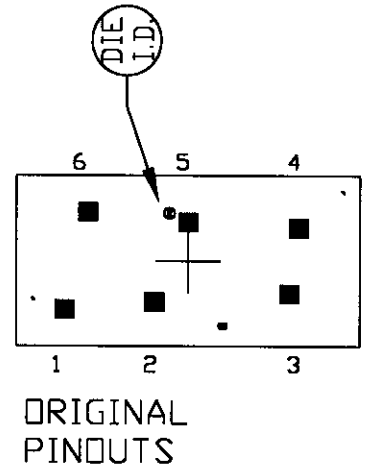
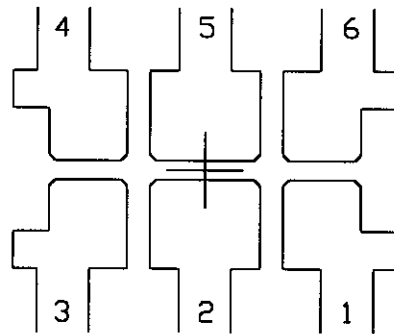
3.4 Pin combinations to be tested.


- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

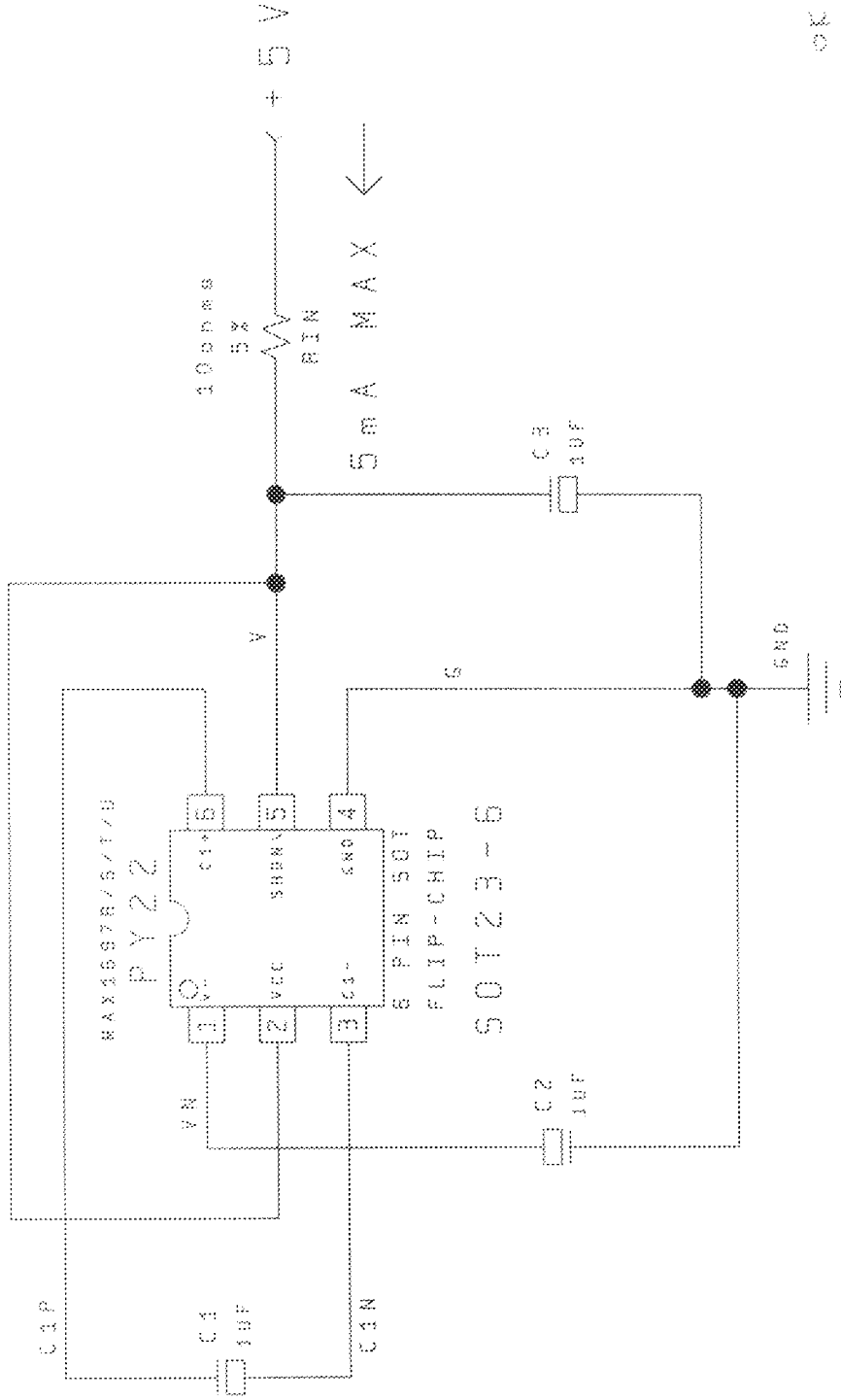


FLIP CHIP PKG.

FLIP LINE



PKG. CODE: U6F-6		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN				BOND DIAGRAM #: 05-2301-0011



OK
SKZ
4/1/99

Doc ID# 06-5436

Note: Use only 1uF ceramic (NON-polarized) capacitors.

MAXIM CONFIDENTIAL	CREATED: 00/00/00	BY: NS	ENG1:	ENG2: -
	LAST SAVED: 4-1-1999, 10:34		SIZE A	REVISION A
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DESC: BURN-IN SCHEMATIC		SHEET 1		OF 1