



ERRATA SHEET

DS3104-SE

Revision A1 Errata

The errata listed below describe situations where DS3104-SE revision A1 components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3104-SE revision A1 components. Revision A1 components are branded on the topside of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively. To obtain an errata sheet on another DS3104-SE die revision, visit our website at www.maxim-ic.com/errata.

1) DIFFERENTIAL INPUT CLOCK IC5 IS NOT FUNCTIONAL

Description:

Differential input clock IC5 is not functional.

Workaround:

None.

2) LVDS/LVPECL CONFIGURATION VALUES REVERSED FOR DIFFERENTIAL OUTPUTS

Description:

For OC4, OC5, OC6, and OC7, the LVDS and LVPECL encodings are reversed in the MCR8 register fields.

Workaround:

To configure an output as LVDS, set the corresponding field in MCR8 to 01b. To configure an output as LVPECL, set the corresponding field to 10b or 11b. (Note that the default signal format is LVPECL for all outputs.) To prepare for this errata being corrected in future revisions, software should check the device revision register REV at address 02h. If REV = 00h (rev A1), the fields of the MCR8 register should be written as described in this errata; otherwise, the fields should be written as described in the data sheet.

3) CANNOT USE DIRECT LOCK MODE FOR 51.84MHz INPUTS

Description:

The Direct Lock Mode for 51.84MHz is not functional.

Workaround:

Use Lock8K Mode or DIVN Lock Mode for inputs configured for 51.84MHz operation.

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4) CANNOT USE LOCK8K MODE FOR 5MHz INPUTS

Description:

The LOCK8K mode for 5MHz is not functional.

Workaround:

Use Direct Lock Mode or DIVN Lock Mode for inputs configured for 5MHz operation.

5) ISSUE WITH READS FROM FREQ AND PHASE REGISTERS

Description:

When reading the FREQ and PHASE multiregister fields over the SPI interface, the last byte read (i.e., the third FREQ register or the second PHASE register read) may be a newer update of the multiregister field than the byte(s) read previously. This issue does not occur when the SPI bus is clocked at 10MHz but can occur at slower SPI clock rates.

Workaround:

One workaround is to clock the SPI bus at 10MHz. One warning about this workaround: rev A2 of the device may have a maximum SPI clock rate less than 10MHz (e.g., 8MHz). To use this workaround, be sure the board can be provisioned for a slower SPI clock rate when a rev A2 device is used.

Another workaround is to read the FREQ and PHASE information from the test registers.

To read T0 DPLL frequency:

- 1) Write 01h to address 0180h.
- 2) Write 01h to address 0186h.
- 3) Read addresses 0181h, 0182h, 0183h, and 0184h (must read all four, in that order) FREQ[18:0] information is in 0181h (LSB), 0182h, and 0183h[2:0] in the same format and units as in the FREQ1, FREQ2, and FREQ3 registers.

To read T0 DPLL phase:

- 1) Write 01h to address 0180h.
- 2) Write 02h to address 0186h.
- 3) Read addresses 0181h, 0182h, 0183h, and 0184h (must read all four, in that order) PHASE[15:0] information is in 0181h (LSB) and 0182h (MSB) in the same format and units as in the PHASE1 and PHASE2 registers.

To read T4 DPLL frequency:

- 1) Write 03h to address 0180h.
- 2) Write 01h to address 0186h.
- 3) Read addresses 0181h, 0182h, 0183h and 0184h (must read all four, in that order) FREQ[18:0] information is in 0181h (LSB), 0182h, and 0183h[2:0] in the same format and units as in the FREQ1, FREQ2, and FREQ3 registers.

To read T4 DPLL phase:

- 1) Write 03h to address 0180h.
- 2) Write 02h to address 0186h.
- 3) Read addresses 0181h, 0182h, 0183h, and 0184h (must read all four, in that order) PHASE[15:0] information is in 0181h (LSB) and 0182h (MSB) in the same format and units as in the PHASE1 and PHASE2 registers.

Note: This workaround will not work unless the device is initialized properly as described in the data sheet. The required initialization file is available at www.maxim-ic.com/DS3104.

6) DEFAULT SIGNAL FORMATS FOR DIFFERENTIAL OUTPUTS

Description:

The reset default values of the OC4SF–OC7SF fields in the MCR8 register are all 10h for rev A1 devices. The actual reset default values should be 00h = disabled for all four fields.

Workaround:

For systems starting with rev A1 parts and migrating to rev A2 parts, software should explicitly configure these register fields to the desired values at system startup and not rely on the reset default values.