



DS3100 Stratum 3/3E Timing Card IC

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REVISION A1 ERRATA

The errata listed below describe situations where DS3100 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3100 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS3100 die revision, visit our website at www.maxim-ic.com/errata.

1. DIFFERENTIAL INPUTS AND OUTPUTS NOT FUNCTIONAL

Description:

Differential input clocks IC5 and IC6 and differential output clocks OC6 and OC7 are not functional.

Work Around:

None.

2. COMPOSITE CLOCK RECEIVERS NOT FUNCTIONAL

Description:

Composite clock receivers IC1A and IC2A are not functional. Input clocks IC1 and IC2 can still be configured for CMOS/TTL operation on input pins IC1 and IC2 by setting MCR5:IC1SF = 1 and MCR5:IC2SF = 1.

Work Around:

None.

3. MULTICYCLE PHASE DETECTOR ISSUE

Description:

The multicycle phase detector (MCPD) can experience cycle slips under certain circumstances and therefore should not be used in applications where input jitter amplitudes are 1 UI or greater.

Work Around:

When tolerance of jitter amplitudes greater than 1 UI is required, use LOCK8K mode or DIVN mode. Use direct lock mode only when input jitter is expected to be less than 1 UI.

4. WRITES TO BITS TRANSCEIVER FRAMERS IN SPI BUS MODE

Description:

In SPI microprocessor interface mode (IFSEL[2:0] = 1X1) writes to addresses 20h through 6Ah in both BITS transceivers are unreliable.

Work Around:

None. Do not use SPI microprocessor interface mode when the BITS transceivers are enabled, or do not use the BITS transceivers when the SPI microprocessor interface is enabled.

5. EXTERNAL REFERENCE SWITCHING MODE NEEDS AT LEAST ONE VALID INPUT CLOCK

Description:

External reference switching mode (MCR10:EXTSW = 1, see Section 7.6.5 in the data sheet) is only enabled when at least one valid input clock is present (PTAB1:REF1! = 0). If there are no valid input clocks then MCR10:EXTSW is ignored, and external reference switching mode is not enabled.

Work Around:

During external reference switching mode set MCR2:T0FORCE to any value other than 0 or 15. This forces PTAB1:REF1 to a nonzero value, allowing external reference switching mode to work correctly. (Since MCR10:EXTSW = 1 has higher priority than MCR2:T0FORCE! = 0, the particular value of MCR2:T0FORCE has no effect on the operation of external reference switching mode.)

6. BITS RECEIVER 6312kHz MODE NOT FUNCTIONAL

Description:

The BITS receivers do not output a clock in 6312kHz mode (BMCR:RMODE[1:0] = 11).

Work Around:

None.

7. PULL-IN TIME AT STRATUM 3E BANDWIDTHS MAY EXCEED REQUIREMENT WHEN USING AUTOBW FEATURE

Description:

When the T0 DPLL is configured for Stratum 3E operation (e.g., T0LBW = 0.0001Hz) and MCR9:AUTOBW = 1 the pull-in time may be > 700 seconds or the DPLL may not pull in, depending on the acquisition bandwidth setting in the T0ABW register.

Work Around:

Two work arounds are being developed. In the first, system software will manually change the DPLL bandwidth over time from a fast acquisition bandwidth through several lower bandwidth steps to a final locked bandwidth setting. In the second workaround, a field update to the DS3100's internal DSP code will be issued. This update will allow the T0 DPLL to perform smooth bandwidth transition from the fast acquisition bandwidth specified by T0ABW to the bandwidth specified by T0LBW without involving system software. Both of these work arounds will be published in future revs of this errata sheet as soon as they are available.

8. BITS TRANSMITTER ANALOG TWEAKS

Description:

In the reset default state the BITS transmitter analog circuitry is not optimally configured.

Work Around:

After setting (or changing) the mode of operation in BMCR:TMODE[1:0], the transmitter line build-out in BLCR2:LBO[2:0] and/or the internal/external impedance setting in BLCR2:TION, follows these steps to optimally configure the analog circuitry:

- 1) Write 01h to address 1FFh.
- 2) Write to the device as shown in the following table.
For BITS transceiver 1, add 190h to the address offsets shown in the table.
For BITS transceiver 2, add 1A0h to the address offsets shown in the table.
- 3) Write 00h to address 1FFh.

OPERATING MODE, LBO AND IMPEDANCE MATCH SETTINGS			ADDRESS OFFSETS TO BE WRITTEN				
BMCR:TMODE	BLCR2:LBO[2:0]	BLCR2:TION	+00h	+02h	+05h	+06h	+07h
DS1	000	X	00h	80h	30h	00h	00h
DS1	001	0	00h	80h	38h	00h	20h
DS1	001	1	A0h	80h	38h	00h	20h
DS1	010	X	00h	80h	30h	00h	20h
DS1	011	0	12h	80h	30h	00h	20h
DS1	011	1	AAh	80h	30h	00h	20h
DS1	100	X	00h	80h	30h	00h	20h
DS1	101	X	00h	AFh	00h	30h	00h
DS1	110	X	00h	A Eh	00h	20h	00h
DS1	111	X	00h	A Eh	00h	00h	00h
E1	000	0	60h	ADh	70h	31h	00h
E1	000	1	00h	ADh	70h	31h	00h
E1	001	0	6Ch	80h	10h	11h	00h
E1	001	1	00h	80h	10h	11h	00h
2048kHz	000	0	60h	B4h	00h	31h	00h
2048kHz	000	1	00h	B4h	00h	31h	00h

9. READY PIN NOT FUNCTIONAL

Description:

In parallel microprocessor interface modes the $\overline{\text{RDY}}$ pin does not function as described in the data sheet.

Work Around:

Ignore the $\overline{\text{RDY}}$ pin. The parallel microprocessor interface can be used in any mode without using $\overline{\text{RDY}}$.