



APPLICATION NOTE 993

Adding Voltage Droop to DDR Memory Termination Voltage Supply Reduces Output Capacitance

Abstract: Power supplies for generating termination voltage supply for DDR memory can tolerate only 40mV variation even during extreme load transients, from the maximum rated sinking current to the maximum rated sourcing current. Typically large expensive capacitors are used to ensure that the tolerance band is not exceeded. But by adding droop to DDR memory termination voltage supply output capacitance can be drastically reduced. This application note illustrates this technique using MAX1917.

The termination voltage supply for DDR memory needs to track the DDR memory supply voltage, VDDQ, and it needs to source and sink the load current. Its maximum voltage deviation should not exceed 40mV during extreme load transients, from the maximum rated sinking current to the maximum rated sourcing current.

The MAX1917 employs a Quick PWM control architecture, which responds to step load change within one switching cycle, resulting in less required output capacitance. By adding intentional voltage droop to the design, output capacitance can be further reduced with no loss in transient performance.

As an example, in a 1.25V/7A termination VTT supply, the output capacitor should be chosen such that the ESR is less than:

$$ESR = \frac{40mV}{2 \times I_o} = \frac{40mV}{2 \times 7A} = 2.85 m\Omega$$

This ESR requirement can be met with five 560µF/4V OSCAN capacitors, or six 270µF/2.5V SPCAPs, or fourteen 150µF/4V POSCAPS at the output. For space considerations, six 270µF/2V SPCAPs were chosen, giving the total ESR of 2.5mΩ. This yields 35mV maximum voltage deviation during a step load change of -7A to 7A to -7A, excluding the output ripple voltage. **Figure 1** shows the schematics of the VTT termination voltage supply.

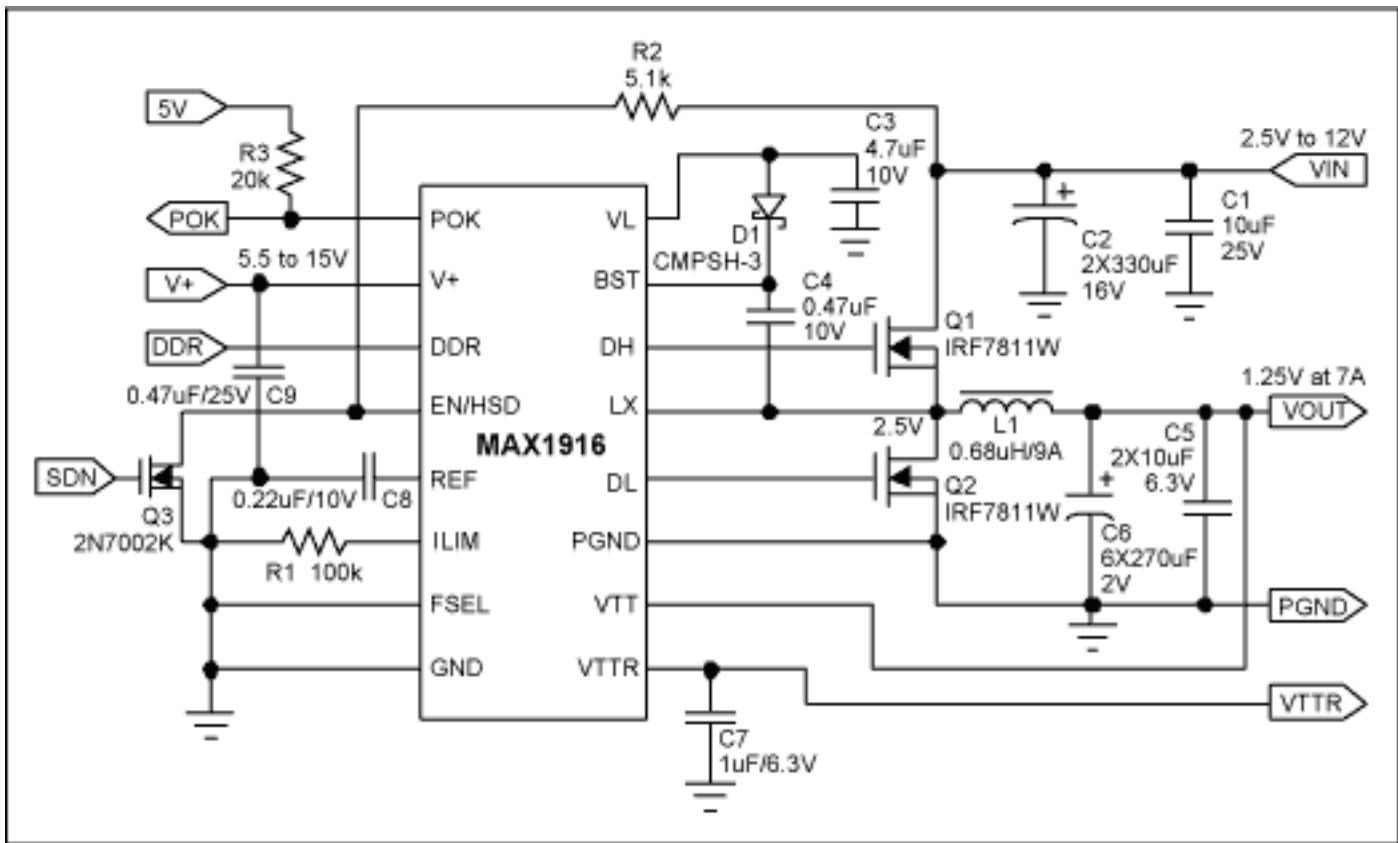


Figure 1. Schematic of 1.25V/7A VTT supply.

Figure 2 shows the waveforms of VTT and output current during step load transients. It is evident from this figure that the maximum voltage deviation is less than 40mV. It is also clear from Figure 2 that the peak voltage overshoot or under shoot ends right after the load transient is finished, indicating a very fast loop response.

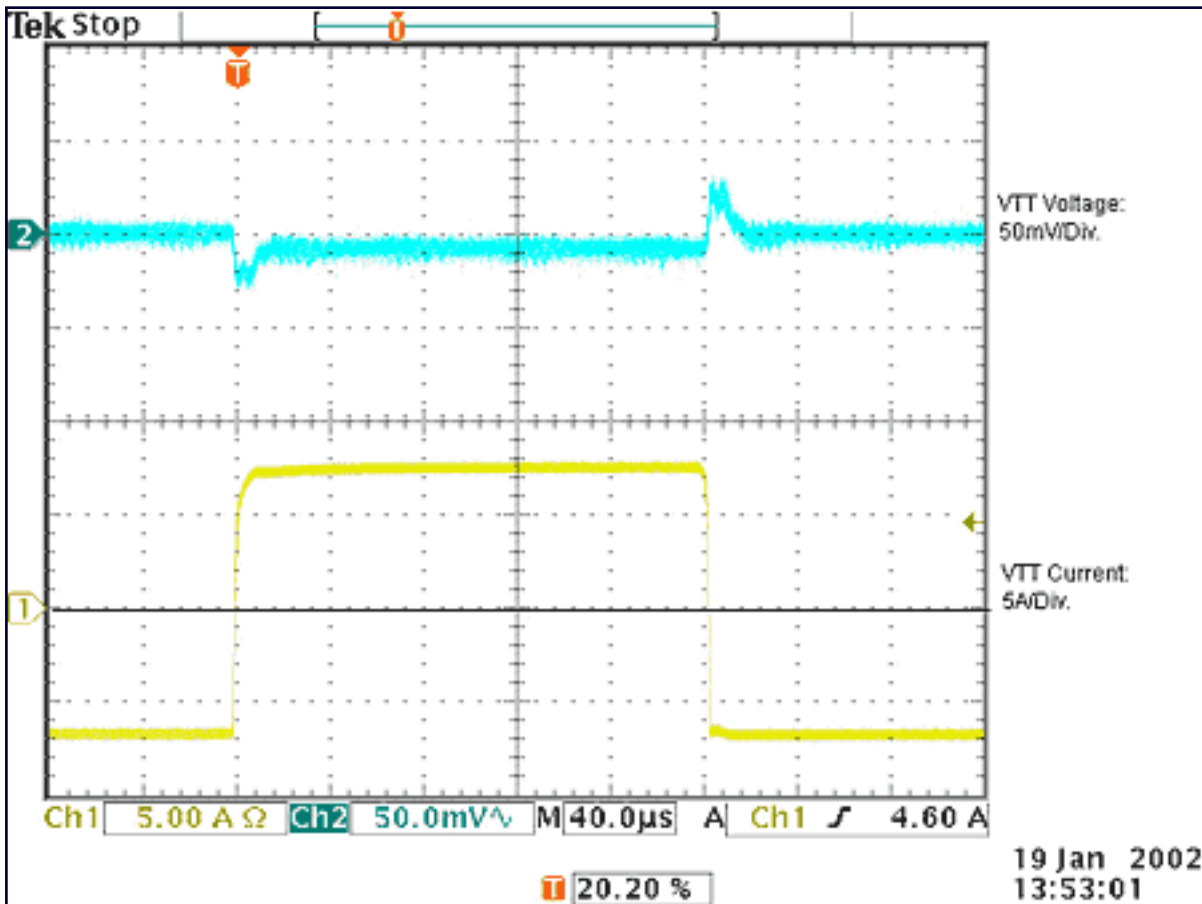


Figure 2. Waveforms of VTT and load current during a step load transient.

When droop method is used the required ESR can be doubled, i.e., 5mΩ from previous calculation. The maximum droop resistance is given by

$$R_{dp} \leq \frac{2 \times 40mV - V_{RIPPLE} - V_{Loadreg}}{2 \times I_O} = \frac{80mV - 10mV - 14mV}{2 \times 7} = 4m\Omega$$

Where V_{Load} is the load regulation, which is about 1mV/A, including trace resistance, and V_{Ripple} is the output ripple voltage. Considering some design margin, a 2mΩ resistor, R3, is chosen as shown in **Figure 3**. Also, four SPCAPs are utilized instead of three for design margin, but 2 fewer caps are needed compared to Figure 1. **Figure 4** shows the waveforms of VTT voltage and load current under the same load transient response. The maximum voltage deviation is well within the 80mV voltage band. In conclusion, adding output droop further reduces the required output capacitor and so does the total system cost.

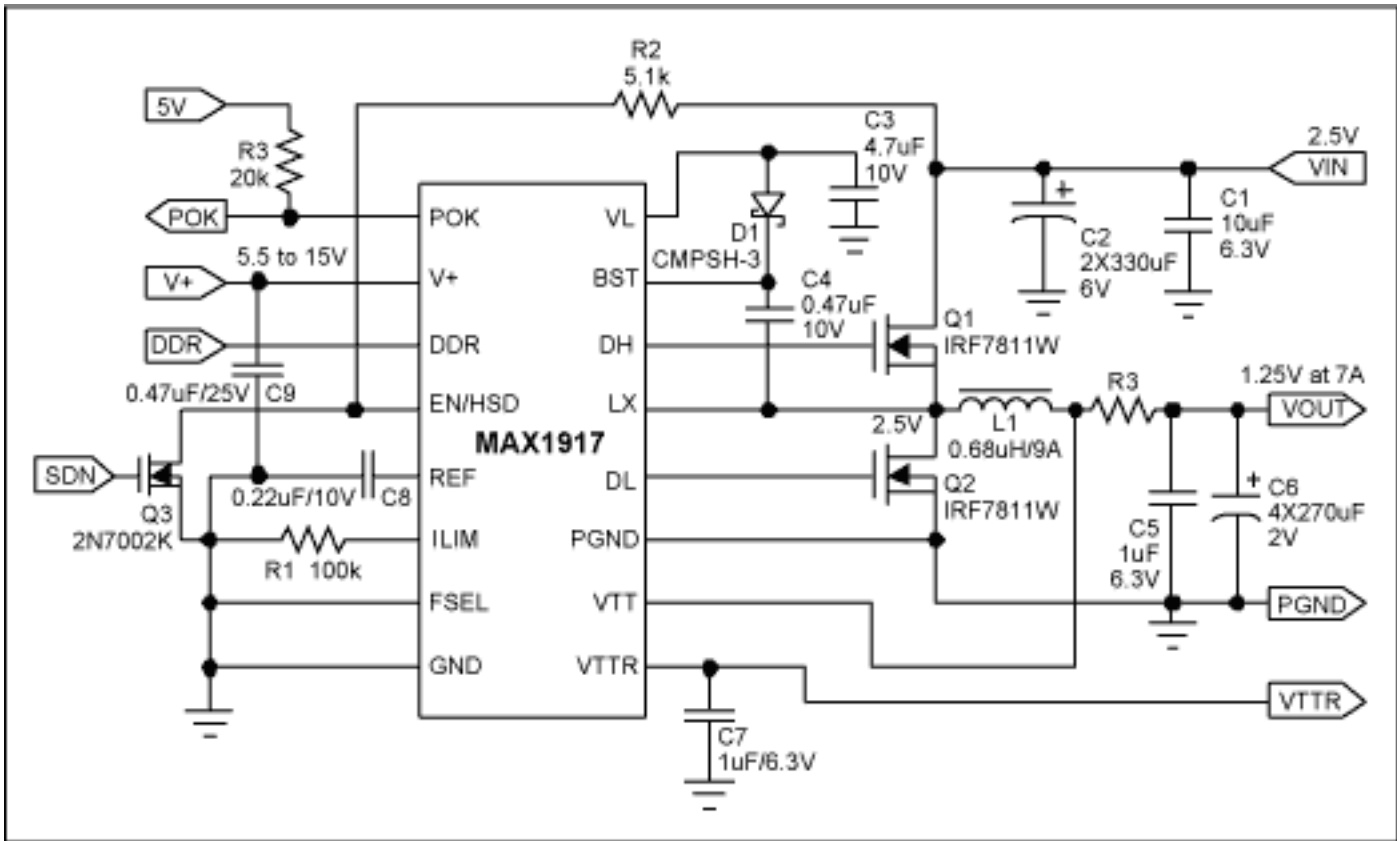


Figure 3. Schematics of VTT supply with output droop.

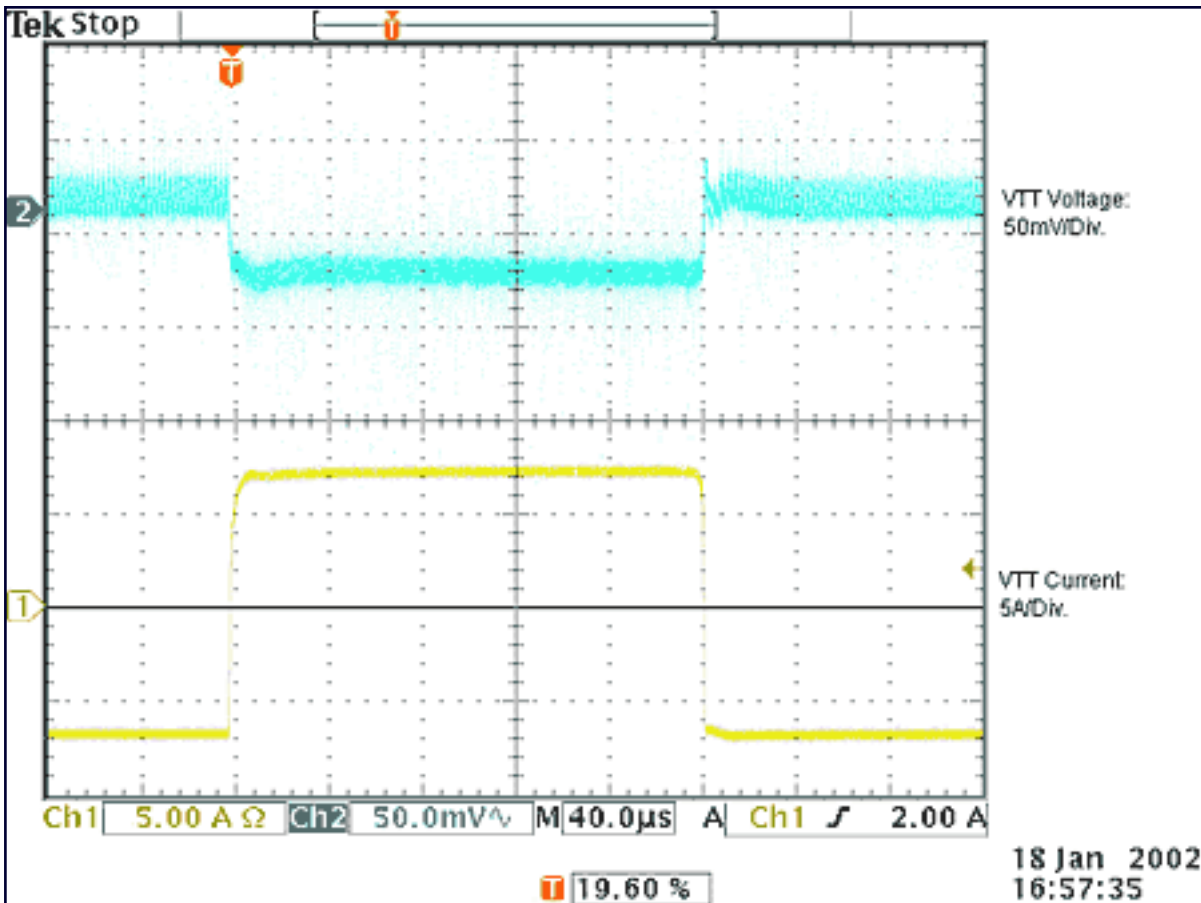


Figure 4. Waveforms of VTT and load current during load transient with output droop.

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MAX1917: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

AN993, AN 993, APP993, Appnote993, Appnote 993

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