



APPLICATION NOTE 646

Semicustom QuickChip ASICs Implement RF Functions to 9GHz

Abstract: Maxim has two different approaches for developing HF ASICs: a semi-custom QuickChip design methodology and the more traditional full-custom design methodology. The semicustom design approach is discussed below and provides a low-cost, fast turn-time approach for developing customer-designed RF ASICs.

In addition to standard product ICs, Maxim offers a rapid-response ASIC service. Semicustom arrays known as "QuickChips" provide designers with a selection of uncommitted semiconductor devices: JFETs, Schottky diodes, ESD-protected diodes, MOS capacitors, trimmable nichrome resistors, and bipolar transistors with f_T s to 27GHz. Completing one of these chips with a custom metal mask set interconnects the selected components to create a high-frequency, high-performance circuit.

A comprehensive set of design, verification, and layout software tools has been developed to ensure a high probability that QuickChip designs will meet their target specifications on the first pass. Both UNIX and PC platforms are supported.

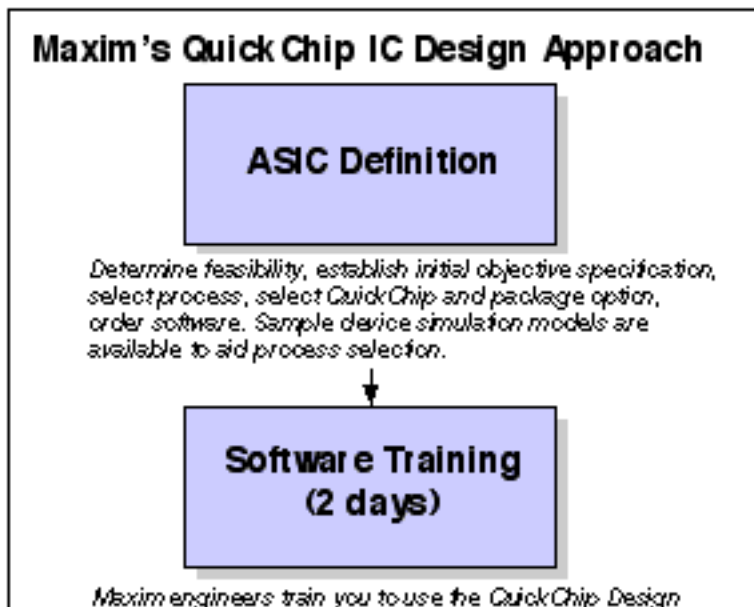
Three different QuickChip families are available. The QC10 family of seven arrays is made with a complementary bipolar process featuring NPN and PNP f_T s of 9GHz and 6GHz, respectively. It is optimized for analog signal acquisition, amplification, and sourcing.

The QC6 family of four arrays is fabricated in a process with 9GHz NPN and 80MHz PNP f_T s. These arrays are suitable for a wide range of fiber, IF, and instrumentation applications.

The QC9 array is fabricated in a 27GHz process and is intended for RF and HF applications. More than 35 designs have been completed using the QC9 array since its introduction. These include a 900MHz transceiver, a 7GHz prescaler, several GPS receivers, an OC48 amp-lifier, pulse and window comparators, and a 2x2 crosspoint switch.

The design examples that follow, reprinted with kind permission of the IEEE, illustrate the capabilities of QuickChip ASICs.

For further information, or to request a copy of Maxim's *High-Frequency ASIC Development Handbook*, contact Maxim's HF ASIC Group, attention Raj Garg, via FAX at 503-547-0810.



**Software Training
(2 days)**

Maxim engineers train you to use the QuickChip Design Tools included in the QuickTools package: Analog Design System (schematic capture and simulator), CuERC (electrical rule checker), and QuickKic (layout editor).

**Design & Layout
(project dependent)**

Design and simulate the circuit, check for electrical rule violations with CuERC, and lay out your circuit design using QuickKic. Maxim reviews both the circuit design and layout

**Tapeout
(2 weeks)**

Maxim performs the final layout versus schematic verification, electrical rule check, and layout design rule check before tapeout. Upon successful completion of final design database verification and a signed customer layout release, Maxim orders masks.

**Wafer Fabrication
(4 weeks, QC6/QC10)
(6 weeks, QC9-60D)**

Maxim fabricates die using 3 to 6 QuickChip nichrome, metal, and via masks.

**Die Prep
& Packaging
(3 weeks)**

Maxim packages untested prototype die. Production testing is available.

**Delivery of
Prototypes**

Prototypes can now be evaluated in your application.

Application Note 646: <http://www.maxim-ic.com/an646>

More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

Other questions and comments: <http://www.maxim-ic.com/contact>

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