



APPLICATION NOTE 592

Silicon Timed Circuits: Frequently Asked Questions

Abstract: The technical brief answers frequently asked questions (FAQs) regarding Dallas Semiconductor silicon timed circuits (STCs), also known as delay lines. This brief discusses both laser-trimmed (older) as well as EEPROM-trimmed (newer) devices. Topics include, decoupling, comparisons to hybrid devices, how delay lines work, replacing older (DS10XX-series) with newer (DS11XX) series delay lines, temperature compensation, evaluating parametric specifications, as well as the availability of custom devices.

Do Silicon Delay Lines Require Decoupling?

Silicon Timed Circuits (STCs) contain noise-sensitive voltage detection circuits and fast rise-time output circuits so decoupling is required. A 0.01 μ f to 0.1 μ f low-inductance capacitor should be used in close proximity to the delay line to assure the highest performance.

What Are the Advantages of STCs Over Hybrid Devices?

STCs offer advantages in design, packaging, and manufacturing over hybrids. Specifically, STCs offer the increased reliability of silicon and greater accuracy on both rising and falling edges. Unlike TTL devices, STCs are CMOS devices and offer true rail-to-rail output levels, which help minimize system standby power requirements. Using standard DIP, SO, μ SOP, and TSSOP packaging, STCs are well-suited to standard IC handling, including reflow soldering.

What Is the Basic Operation of an STC?

Presently, two architectures are used to implement delay lines. The first uses a ramp generator and associated logic to generate the delay period. The input signal triggers a ramp generator that is compared to a laser-adjusted voltage reference. When the ramp regenerator reaches the preset voltage level, the delay period is determined. The second architecture uses a chain of temperature- and voltage-compensated voltage controlled delay lines (VCDL) to develop the total delay period. We are in the process of converting all delay lines from the first architecture to the second, much improved architecture. The DS10XX series of delay lines are made up of the old architecture. The DS11XX will gradually replace the older series with pin-for-pin replacements in most cases. The new architecture also permits us to put the delay lines in smaller packages such as the 8-pin μ SOP (MicroMax) which is half the size of the 8-pin SO package. We have already introduced the DS1100 series as replacements for the DS1000 series and the DS1135 series as replacements for the DS1035/DS1033 series. The DS1110 series is a replacement for the DS1010 series.

How Do I Know Which DS1100 Series to Use as a Replacement for the DS1000 Series?

The following table can be used to cross-reference the old part numbers to the new. Some older packages such as gullwing and sheared-lead packages will not have drop-in but functional replacements. The DS1000M-500 and DS1000Z-500 will continue to be available.

Obsolete Part Number	Package Type	Number of Pins	Suggested Replacement Part Number	Package Type	Number of Pins	Replaces Function	Replaces Package
DS1000-xxx	DIP	14-PIN	DS1100M-xxx	DIP	8-PIN	Yes	No
DS1000M-xxx	DIP	8-PIN	DS1100M-xxx	DIP	8-PIN	Yes	Yes
DS1000G-xxx	Gullwing	14-PIN	DS1100Z-xxx	SO	8-PIN	Yes	No
DS1000H-xxx	Gullwing	8-PIN	DS1100Z-xxx	SO	8-PIN	Yes	No
DS1000K-xxx	N/C Leads Sheared	14-PIN	DS1100M-xxx	DIP	8-PIN	Yes	No
DS1000S-xxx	SO	16-PIN	DS1100Z-xxx	SO	8-PIN	Yes	No
DS1000Z-xxx	SO	8-PIN	DS1100Z-xxx	SO	8-PIN	Yes	Yes
DS1000-xxx IND	DIP	14-PIN	DS1100Z-xxx	DIP	8-PIN	Yes	No
DS1000M-xxx IND	DIP	8-PIN	DS1100M-xxx	DIP	8-PIN	Yes	Yes
DS1000S-xxx IND	SO	16-PIN	DS1100Z-xxx	SO	8-PIN	Yes	No
DS1000Z-xxx IND	SO	8-PIN	DS1100Z-xxx	SO	8-PIN	Yes	Yes

Notes:

1. Gullwing, sheared lead and 16-pin SO will not be available in the DS1100 family.
2. DS1100 family is qualified for both commercial and industrial temperature ranges.

How Do I Know Which DS1135 Series to Use as a Replacement for the DS1035 Series?

Devices Affected (All Parts Are Direct Replacements)

Obsolete Part Number	Delay Length (ns)	Package	Replacement Part Number
DS1035M-6	6	8-PIN DIP	DS1135M-6
DS1035M-8	8	8-PIN DIP	DS1135M-8
DS1035M-10	10	8-PIN DIP	DS1135M-10
DS1035M-12	12	8-PIN DIP	DS1135M-12
DS1035M-15	15	8-PIN DIP	DS1135M-15
DS1035M-20	20	8-PIN DIP	DS1135M-20
DS1035M-25	25	8-PIN DIP	DS1135M-25
DS1035M-30	30	8-PIN DIP	DS1135M-30
DS1035Z-6/T&R	6	8-PIN SO T&R	DS1135Z-6 T&R
DS1035Z-8/T&R	8	8-PIN SO T&R	DS1135Z-8 T&R
DS1035Z-10/T&R	10	8-PIN SO T&R	DS1135Z-10/T&R
DS1035Z-12/T&R	12	8-PIN SO T&R	DS1135Z-12/T&R
DS1035Z-15/T&R	15	8-PIN SO T&R	DS1135Z-15/T&R
DS1035Z-20/T&R	20	8-PIN SO T&R	DS1135Z-20/T&R
DS1035Z-25/T&R	25	8-PIN SO T&R	DS1135Z-25/T&R
DS1035Z-30/T&R	30	8-PIN SO T&R	DS1135Z-30/T&R
DS1035Z-6	6	8-PIN SO	DS1135Z-6
DS1035Z-8	8	8-PIN SO	DS1135Z-8
DS1035Z-10	10	8-PIN SO	DS1135Z-10
DS1035Z-12	12	8-PIN SO	DS1135Z-12
DS1035Z-15	15	8-PIN SO	DS1135Z-15
DS1035Z-20	20	8-PIN SO	DS1135Z-20
DS1035Z-25	25	8-PIN SO	DS1135Z-25
DS1035Z-30	30	8-PIN SO	DS1135Z-30
DS1035C-601	6	8-PIN SO T&R	DS1135Z-6 /T&R
DS1035C-602	8	8-PIN SO T&R	DS1135Z-8/T&R
DS1035C-701	8	8-PIN SO T&R	DS1135Z-8/T&R
DS1035C-702	6	8-PIN SO T&R	DS1135Z-6/T&R
DS1035Z-901	20	8-PIN SO T&R	DS1135Z-20/T&R

DS1135 is qualified over the commercial as well as the industrial temperature range. No separate industrial part number is required.

What About the DS1033? I Don't See a DS1133 Replacement.

The DS1135L series replaces the DS1033 series. Not all packages have drop-in replacements. Refer to the table below to select either a functional or drop-in replacement.

Devices Affected

Ordering Part Number	Delay (ns)	Package	Replacement Part No.	Functional Replacement
DS1033C-803	15	8-PIN SO	DS1135LZ-15	
DS1033C-803/T&R	15	8-PIN SO/T&R	DS1135LZ-15/T&R	
DS1033C-902	8	8-PIN SO	NOT OBSOLETE	
DS1033C-902/T&R	8	8-PIN SO/T&R	NOT OBSOLETE	
DS1033M-10	10	8-PIN DIP	OBSOLETE	DS1135LZ-10
DS1033M-12	12	8-PIN DIP	OBSOLETE	DS1135LZ-12
DS1033M-15	15	8-PIN DIP	OBSOLETE	DS1135LZ-15
DS1033M-20	20	8-PIN DIP	OBSOLETE	DS1035LZ-20
DS1033M-25	25	8-PIN DIP	OBSOLETE	DS1135LZ-25
DS1033M-30	30	8-PIN DIP	OBSOLETE	DS1135LZ-30
DS1033M-8	8	8-PIN DIP	OBSOLETE	DS1033Z-8
DS1033Z/T&R	20	8-PIN SO/T&R	DS1135LZ-20/T&R	
DS1033Z-10	10	8-PIN SO	DS1135LZ-10	
DS1033Z-10/T&R	10	8-PIN SO/T&R	DS1135LZ-10/T&R	
DS1033Z-12	12	8-PIN SO	DS1135LZ-12	
DS1033Z-12/T&R	12	8-PIN SO/T&R	DS1135LZ-12/T&R	
DS1033Z-15	15	8-PIN SO	DS1135LZ-15	
DS1033Z-15/T&R	15	8-PIN SO/T&R	DS1135LZ-15/T&R	
DS1033Z-20	20	8-PIN SO	DS1135LZ-20	
DS1033Z-25	25	8-PIN SO	DS1135LZ-25	
DS1033Z-25/T&R	25	8-PIN SO/T&R	DS1135LZ-25/T&R	
DS1033Z-25/T&R/	25	8-PIN SO/T&R	DS1135LZ-25/T&R	
DS1033Z-30	30	8-PIN SO	DS1135LZ-30	
DS1033Z-8	8	8-PIN SO	NOT OBSOLETE	
DS1033Z-8/T&R/	8	8-PIN SO/T&R	NOT OBSOLETE	
DS1033Z-8/T&R	8	8-PIN SO/T&R	NOT OBSOLETE	

DS1135L is qualified over the commercial as well as the industrial temperature range. No separate industrial part number is required.

How Do I Correlate Time Measurements When Evaluating Delay Lines?

Fast (3ns) rise/fall input pulses with 0V to 3V logic levels, low inductance decoupling techniques using 0.01 μ f to

0.1 μ f capacitors, low capacitance measurement probes placed as close as possible to the package, and relaxed timing (500ns pulse width, 1 μ s period) will aid in timing correlation when measured at 1.5V levels.

Can I Get Any Delay Time I Need From Dallas Semiconductor?

Yes, delay lines can be customized to meet your design timing requirements. We can even supply sample quantities in ceramic packages for evaluation.

Do STCs Need To Be Compensated for Temperature Like Hybrids?

On STCs, temperature compensation is implemented by balancing the positive temperature coefficient of the CMOS logic against the negative coefficient elements in the device. These two effects tend to cancel each other, minimizing the effects of temperature. Rather than measuring the coefficients in parts per million, silicon delay lines are measured as the maximum shift from nominal, anywhere along the rated temperature range.

Can I Add or Daisy-Chain Several Devices to Achieve a Longer Delay?

Daisy-chaining silicon delay lines presents a problem that is increased with the number of packages in a chain. A voltage-chopped stabilization circuit in the design causes a slight time jitter (well within specifications and almost transparent to the circuit) on the output. When the packages are daisy-chained, the jitter is cumulative and degrades the accuracy of downline stages. If four to six packages are chained in a series, the results are generally unacceptable.

How Do STCs Differ From Hybrid Devices?

A typical hybrid consists of a hex inverter die, a PC board acting as a ground plane, plus chip capacitors, a terminating resistor, and a multiple tap ferrite inductor. Timing is determined by coil winding and/or capacitor selection or trimming. The Dallas Semiconductor STC design uses a laser- or EEPROM-optimized die bonded to a conventional lead frame, which is then molded into an auto-insertable DIP, or SO, μ SOP, or TSSOP package.

Can an STC Be Used To Time-Shift a Square Wave?

Yes, it's a good solution. Just be certain that the minimum input period specification is met.

Why Is the Static (Idle) Current So High?

Unlike typical CMOS devices, which offer minimal static current, most Dallas Semiconductor delay lines draw almost as much current when idling as when active. This is because the constant-current sources in the timing circuits are always on. If they were turned off in the absence of an input pulse, the time required to establish a stable reference current when the next pulse arrives would impair the accuracy of the device.

How Does Laser Adjustment Trim the Delay?

Under the direction of a computer-controlled tester with 20-picosecond resolution, the proper time delay of the device is set by two means. In the first, directing a laser to open polysilicon fuses, removing unnecessary current sources and capacitors in ramp generators in the timing circuit. This technique is used on earlier generations of the parts and is gradually being phased out. Newer architecture parts use EEPROM to engage positive and negative temperature coefficient timing elements in the delay circuitry setting the delay time and balancing the components in such a manner that parametric changes over temperature null each other out.

What About Daisy-Chaining the Stages of a Parallel STC?

With the exception of the fast taps on the DS1007, some jitter will be added with each stage when added in a series. This will not be a problem in most cases. Users report that daisy-chaining this way is a convenient method of implementing non-standard delay times

Application Note 592: <http://www.maxim-ic.com/an592>

More Information

For technical questions and support: <http://www.maxim-ic.com/support>

For samples: <http://www.maxim-ic.com/samples>

Other questions and comments: <http://www.maxim-ic.com/contact>

Related Parts

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DS1010: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS1013: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

DS1020: [QuickView](#) -- [Full \(PDF\) Data Sheet](#) -- [Free Samples](#)

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