



APPLICATION NOTE 4199

Porting Applications from the High-Speed Micro Family to Ultra-High-Speed Flash Microcontrollers

Abstract: There are many reasons to upgrade older 8051 designs that use high-speed microcontrollers (DS80C310/DS80C320/DS80C323/DS8xC520) to the newer ultra-high-speed flash microcontrollers (DS89C430/DS89C450). Incentives to upgrade include higher performance, additional features and peripherals, and the flexibility of internal flash memory. This application note discusses some important differences between the two microcontroller families and explains how to upgrade from the high-speed to the ultra-high-speed devices.

Overview

Maxim's high-speed microcontroller family includes a wide variety of 8051 microcontrollers which execute instructions at a faster 4 clocks-per-machine-cycle rate compared to the 8051's original 12 clocks-per-machine cycle speed. Some of the high-speed microcontrollers operate entirely from external program memory, such as the DS80C310, while others contain internal EPROM or ROM program memory, such as the DS87C520/DS83C520. All of these high-speed devices are pin-compatible with existing 8051 microcontrollers, so designs can be upgraded in most cases simply by dropping in a faster device and making minor software adjustments.

In a similar manner, the ultra-high-speed flash microcontrollers can be used as drop-in upgrades for high-speed microcontroller designs. These newer, more powerful microcontrollers, which include the DS89C430/DS89C450, offer important improvements: expanded internal program flash memory (up to 64kB); and a redesigned, ultra-high-speed microcontroller core capable of executing instructions in a single clock cycle for up to a 12x speed improvement over the original 8051 design.

This application note discusses how to upgrade from the high-speed microcontrollers to ultra-high-speed flash devices. The article also outlines differences in feature sets, pinout details, and SFR changes that must be considered when upgrading a design.

General References

For general programming guidelines for the following devices, consult the [High-Speed Microcontroller User's Guide](#) (PDF).

- [DS80C310 High-Speed Microcontroller](#)
- [DS80C320 High-Speed Low-Power Microcontroller](#)
- [DS80C323 High-Speed Low-Power Microcontroller](#)
- [DS83C520 High-Speed ROM Microcontroller](#)
- [DS87C520 High-Speed EPROM Microcontroller](#)

For general programming guidelines for the following devices, consult the [Ultra-High-Speed Flash Microcontroller User's Guide](#) (PDF).

- [DS89C430 Ultra-High-Speed Flash Microcontroller](#)

- [DS89C450 Ultra-High-Speed Flash Microcontroller](#)

Basic Device Features

Table 1. Comparison of Device Features

Feature	DS80C310	DS80C320 DS80C323	DS87C520 DS83C520	DS89C430 DS89C450
Clocks per Machine Cycle	4	4	4	1
Operating Voltage Range (V)	4.5 to 5.5	4.25 to 5.5 (DS80C320) 2.7 to 5.5 (DS80C323)	4.5 to 5.5	4.5 to 5.5
Clock Rate (MHz, max)	33	33 (DS80C320) 18 (DS80C323)	33	33
Instruction Execution Time (ns, min)	121	121 (DS80C320) 222 (DS80C323)	121	30
Crystal Multiplier				√ (x2 or x4)
Ring Oscillator		√	√	√
Internal Program Memory	None	None	16kB	16kB (DS89C430) 64kB (DS89C450)
Internal Register Memory (Bytes)	256	256	256	256
Internal MOVX Memory	None	None	1kB	1kB
Serial Ports (UARTs)	1	2	2	2
External Interrupts	6	6	6	6
Port Pins (with Bus Active)	16	16	16	16
Port Pins (max)	16	16	32	32
Timer/Counters	Three/16-bit	Three/16-bit	Three/16-bit	Three/16-bit
Watchdog		√	√	√
Dual Data Pointers	√	√	√	√
Autoincrement/Decrement				√
Stop Mode	√	√	√	√
Power-On Reset	√	√	√	√
Power-Fail Interrupt		√	√	√

Device Pinout Scheme

Table 2. Device Pinout Differences

DIP	PLCC	TQFP	DS80C310	DS80C320 DS80C323	DS87C520 DS83C520	DS89C430 DS89C450
1	2	40	P1.0 (T2)	P1.0 (T2)	P1.0 (T2)	P1.0 (T2)
2	3	41	P1.1 (T2EX)	P1.1 (T2EX)	P1.1 (T2EX)	P1.1 (T2EX)
3	4	42	P1.2	P1.2 (RXD1)	P1.2 (RXD1)	P1.2 (RXD1)
4	5	43	P1.3	P1.3 (TXD1)	P1.3 (TXD1)	P1.3 (TXD1)
5	6	44	P1.4 (INT2)	P1.4 (INT2)	P1.4 (INT2)	P1.4 (INT2)
6	7	1	P1.5 (nINT3)	P1.5 (nINT3)	P1.5 (nINT3)	P1.5 (nINT3)
7	8	2	P1.6 (INT4)	P1.6 (INT4)	P1.6 (INT4)	P1.6 (INT4)
8	9	3	P1.7 (nINT5)	P1.7 (nINT5)	P1.7 (nINT5)	P1.7 (nINT5)
9	10	4	RST	RST	RST	RST
10	11	5	P3.0 (RXD0)	P3.0 (RXD0)	P3.0 (RXD0)	P3.0 (RXD0)
11	13	7	P3.1 (TXD0)	P3.1 (TXD0)	P3.1 (TXD0)	P3.1 (TXD0)
12	14	8	P3.2 (nINT0)	P3.2 (nINT0)	P3.2 (nINT0)	P3.2 (nINT0)
13	15	9	P3.3 (nINT1)	P3.3 (nINT1)	P3.3 (nINT1)	P3.3 (nINT1)
14	16	10	P3.4 (T0)	P3.4 (T0)	P3.4 (T0)	P3.4 (T0)
15	17	11	P3.5 (T1)	P3.5 (T1)	P3.5 (T1)	P3.5 (T1)
16	18	12	P3.6 (nWR)	P3.6 (nWR)	P3.6 (nWR)	P3.6 (nWR)
17	19	13	P3.7 (nRD)	P3.7 (nRD)	P3.7 (nRD)	P3.7 (nRD)
18	20	14	XTAL2	XTAL2	XTAL2	XTAL2
19	21	15	XTAL1	XTAL1	XTAL1	XTAL1
20	22, 23	16, 17	GND	GND	GND	GND
–	1	39	GND	N/C (can be connected to GND if desired)	GND	GND
21	24	18	A8 (P2.0)	A8 (P2.0)	A8 (P2.0)	A8 (P2.0)
22	25	19	A9 (P2.1)	A9 (P2.1)	A9 (P2.1)	A9 (P2.1)
23	26	20	A10 (P2.2)	A10 (P2.2)	A10 (P2.2)	A10 (P2.2)
24	27	21	A11 (P2.3)	A11 (P2.3)	A11 (P2.3)	A11 (P2.3)
25	28	22	A12 (P2.4)	A12 (P2.4)	A12 (P2.4)	A12 (P2.4)
26	29	23	A13 (P2.5)	A13 (P2.5)	A13 (P2.5)	A13 (P2.5)
27	30	24	A14 (P2.6)	A14 (P2.6)	A14 (P2.6)	A14 (P2.6)
28	31	25	A15 (P2.7)	A15 (P2.7)	A15 (P2.7)	A15 (P2.7)
29	32	26	nPSEN	nPSEN	nPSEN	nPSEN
30	33	27	ALE	ALE	ALE	ALE/nPROG
31	35	29	nEA	nEA	nEA	nEA
32	36	30	AD7	AD7	AD7 (P0.7)	AD7 (P0.7)
33	37	31	AD6	AD6	AD6 (P0.6)	AD6 (P0.6)
34	38	32	AD5	AD5	AD5 (P0.5)	AD5 (P0.5)
35	39	33	AD4	AD4	AD4 (P0.4)	AD4 (P0.4)
36	40	34	AD3	AD3	AD3 (P0.3)	AD3 (P0.3)
37	41	35	AD2	AD2	AD2 (P0.2)	AD2 (P0.2)

38	42	36	AD1	AD1	AD1 (P0.1)	AD1 (P0.1)
39	43	37	ADO	ADO	ADO (P0.0)	ADO (P0.0)
40	44	38	V _{CC} (+5V)	V _{CC} +5V (DS80C320) V _{CC} +3V (DS80C323)	V _{CC} (+5V)	V _{CC} (+5V)
–	12	6	N/C	N/C	N/C	V _{CC} (+5V)
–	34	28	N/C	N/C	N/C	GND

Device Registers

Table 3. SFR Map Comparisons

Address	DS80C310	DS80C320 DS80C323	DS87C520 DS83C520	DS89C430 DS89C450
80h	–	–	P0	P0
81h	SP	SP	SP	SP
82h	DPL	DPL	DPL	DPL
83h	DPH	DPH	DPH	DPH
84h	DPL1	DPL1	DPL1	DPL1
85h	DPH1	DPH1	DPH1	DPH1
86h	DPS	DPS	DPS	DPS
87h	PCON	PCON	PCON	PCON
88h	TCON	TCON	TCON	TCON
89h	TMOD	TMOD	TMOD	TMOD
8Ah	TL0	TL0	TL0	TL0
8Bh	TL1	TL1	TL1	TL1
8Ch	TH0	TH0	TH0	TH0
8Dh	TH1	TH1	TH1	TH1
8Eh	CKCON	CKCON	CKCON	CKCON
90h	P1	P1	P1	P1
91h	EXIF	EXIF	EXIF	EXIF
96h	–	–	–	CKMOD
98h	SCON	SCON0	SCON0	SCON0
99h	SBUF	SBUF0	SBUF0	SBUF0
9Dh	–	–	–	ACON
A0h	P2	P2	P2	P2
A8h	IE	IE	IE	IE
A9h	SADDR0	SADDR0	SADDR0	SADDR0
AAh	–	SADDR1	SADDR1	SADDR1
B0h	P3	P3	P3	P3
B1h	–	–	–	IP1
B8h	IP	IP	IP	IP0
B9h	SADEN0	SADEN0	SADEN0	SADEN0
BAh	–	SADEN1	SADEN1	SADEN1

C0h	–	SCON1	SCON1	SCON1
C1h	–	SBUF1	SBUF1	SBUF1
C2h	–	–	ROMSIZE	ROMSIZE
C4h	–	–	PMR	PMR
C5h	STATUS	STATUS	STATUS	STATUS
C7h	–	TA	TA	TA
C8h	T2CON	T2CON	T2CON	T2CON
C9h	T2MOD	T2MOD	T2MOD	T2MOD
CAh	RCAP2L	RCAP2L	RCAP2L	RCAP2L
CBh	RCAP2H	RCAP2H	RCAP2H	RCAP2H
CCh	TL2	TL2	TL2	TL2
CDh	TH2	TH2	TH2	TH2
DOh	PSW	PSW	PSW	PSW
D5h	–	–	–	FCNTL
D6h	–	–	–	FDATA
D8h	WDCON	WDCON	WDCON	WDCON
E0h	ACC	ACC	ACC	ACC
E8h	EIE	EIE	EIE	EIE
F0h	B	B	B	B
F1h	–	–	–	EIP1
F8h	EIP	EIP	EIP	EIP0

Table 4. SFR Function Differences

SFR	Bit(s)	Differences
P0	–	DS8xC520/DS89C430/DS89C450 only; controls Port 0 pins.
DPS	4 (AID)	DS89C430/DS89C450 only; controls the autoincrement/decrement function for the active data pointer.
	5 (TSL)	DS89C430/DS89C450 only; enables automatic toggling between data pointers after certain opcodes.
	6 (ID0)	DS89C430/DS89C450 only; controls the effect of INC DPTR (increment or decrement) on DPTR.
	7 (ID1)	DS89C430/DS89C450 only; controls the effect of INC DPTR (increment or decrement) on DPTR1.
PCON	4 (OFDE)	DS89C430/DS89C450 only; crystal oscillator fail detection enable.
	5 (OFDF)	DS89C430/DS89C450 only; crystal oscillator fail detection flag.
CKCON	7 (WD1) 6 (WD0)	On all devices except the DS80C310; these bits control the watchdog timer period.
EXIF	0 (BGS)	On all devices except the DS80C310; this bit enables/disables the bandgap reference during stop mode.
	1 (RGSL)	On all devices except the DS80C310; this bit controls execution from the ring oscillator during the crystal warmup period.
	2 (RGMD)	On all devices except the DS80C310; this flag indicates the current clock source (ring or crystal).
	3	DS8xC520 (XT/nRG); selects the ring oscillator or crystal as the desired clock source. DS89C430/DS89C450 (CKRY); indicates that the crystal oscillator or crystal multiplier has completed its warmup period.

CKMOD	3 (T0MH)	DS89C430/DS89C450 only; allows Timer 0 to run directly from the system clock (clock/1).
	4 (T1MH)	DS89C430/DS89C450 only; allows Timer 1 to run directly from the system clock (clock/1).
	5 (T2MH)	DS89C430/DS89C450 only; allows Timer 2 to run directly from the system clock (clock/1).
ACON	5 (PAGES0) 6 (PAGES1)	DS89C430/DS89C450 only; selects the page-mode configuration for external bus operations.
	7 (PAGEE)	DS89C430/DS89C450 only; enables page mode (as opposed to the standard 8051 expanded bus mode) for external bus operations.
IE	6 (ES1)	On all devices except the DS80C310; this bit enables/disables the serial port 1 interrupt.
SADDR1	–	On all devices except the DS80C310; this register controls the slave address for serial port 1.
IP1	–	DS89C430/DS89C450 only; this register combines with the settings in IPO/IP to provide four priority-level settings for each interrupt (as opposed to two settings with IP only).
SADEN1	–	On all devices except the DS80C310; this register sets the slave address mask for serial port 1.
SCON1	–	On all devices except the DS80C310; this register controls mode settings for serial port 1.
SBUF1	–	On all devices except the DS80C310; this register provides the input/output buffer for serial port 1.
ROMSIZE	2:0 (RMS2:0)	DS8xC520/DS89C430/DS89C450 only; selects the range of on-chip EPROM/flash that maps into program space.
	3 (PRAME)	DS89C430/DS89C450 only; enables/disables mapping of the 1kB internal RAM into program space.
PMR	1:0 (DME1:0)	DS8xC520/DS89C430/DS89C450 only; controls mapping of internal data memory into data space.
	2	DS8xC520 (ALEOFF); when set to 1, disables ALE during on-board memory access. DS89C430/DS89C450 (ALEON); when set to 0, disables ALE during on-board memory access.
	3	DS8xC520 (XTOFF); when set to 1, disables the crystal oscillator (must run from ring). DS89C430/DS89C450 (4X/n2X); sets the mode for the crystal multiplier.
	4 (CTM)	DS89C430/DS89C450 only; when set to 1, enables the crystal multiplier.
	5 (SWB)	DS8xC520/DS89C430/DS89C450 only; when set to 1, enables automatic switchback mode.
	7:6 (CD1:0)	DS8xC520/DS89C430/DS89C450 only; controls the clock division or multiplier mode. Note that the available settings are different on the DS8xC520/DS89C430/DS89C450.
STATUS	0 (SPRA0)	DS8xC520/DS89C430/DS89C450 only; indicates that a character is currently being received on serial port 0.
	1 (SPTA0)	DS8xC520/DS89C430/DS89C450 only; indicates that a character is currently being transmitted on serial port 0.
	2 (SPRA1)	DS8xC520/DS89C430/DS89C450 only; indicates that a character is currently being received on serial port 1.
	3 (SPTA1)	DS8xC520/DS89C430/DS89C450 only; indicates that a character is currently being transmitted on serial port 1.
	4 (XTUP)	DS8xC520 only; indicates whether the crystal oscillator has completed its warmup cycle.

	5 (LIP)	DS80C320/DS80C323/DS8xC520 only; indicates that a low-priority interrupt is currently being serviced.
	6 (HIP)	DS80C320/DS80C323/DS8xC520 only; indicates that a high-priority interrupt is currently being serviced.
	7 (PIP)	DS80C320/DS80C323/DS8xC520 only; indicates that a power-fail priority interrupt is currently being serviced.
	7:5 (PIS2:0)	DS89C430/DS89C450 only; indicates that the priority level of the interrupt is being serviced.
TA	–	On all except the DS80C310; controls the Timed Access register protection mechanism.
WDCON	0 (RWT)	On all devices except the DS80C310; resets the watchdog timer.
	1 (EWT)	On all devices except the DS80C310; enables/disables the watchdog timer.
	2 (WTRF)	On all devices except the DS80C310; indicates that a watchdog timer reset has occurred.
	3 (WDIF)	On all devices except the DS80C310; indicates that a watchdog timer interrupt has occurred.
	4 (PFI)	On all devices except the DS80C310; indicates that a power-fail interrupt has occurred.
	5 (EPFI)	On all devices except the DS80C310; enables/disables the power-fail interrupt.
	6 (POR)	On all devices; indicates that a power-on reset has occurred.
	7 (SMOD_1)	On all devices except the DS80C310; enables/disables baud-rate doubling mode for serial port 1.
EIE	4 (EWDI)	On all devices except the DS80C310; enables/disables interrupts from the watchdog timer.
EIP	3:0 (PX5:2)	On all devices except the DS89C430/DS89C450; sets high/low priority for external interrupts 2, 3, 4, and 5.
	4 (PWDI)	DS80C320/DS80C323/DS8xC520 only; sets high/low priority for the watchdog timer interrupt.
EIP1, EIP0	–	DS89C430/DS89C450 only; these registers set priority levels 0–3 for the watchdog timer interrupt and external interrupts 2, 3, 4, and 5.

Single-Cycle Execution

The ultra-high-speed DS89C430/DS89C450 processors require only a single clock to execute a single-cycle instruction, which is a 4x speed improvement over the DS80C310/DS80C320/DS80C323/DS8xC520. These latter high-speed microcontrollers require 4 clocks to complete a machine cycle. This difference in clock speed means that simply replacing one of the high-speed devices with the DS89C430/DS89C450 will result in up to a 4x increase in execution speed at the same crystal frequency.

Nonvolatile Memory

The DS80C310/DS80C320/DS80C323 have no programmable internal code memory and require external memory for code storage. The DS8xC520 improves on this memory scheme by including 16kB of program EPROM.

When porting from the DS80C310/DS80C320/DS80C323 to the DS89C430/DS89C450, application code that was stored in external ROM, flash, or EPROM memory can be relocated to the internal flash memory of the ultra-high-speed processors. The DS89C430 provides the same amount of internal program memory (16kB) as the DS8xC520, so any applications stored in the DS8xC520 should fit into the DS89C430 without modification. Applications stored in external program memory will fit in the 64kB internal flash memory of the DS89C450, as

long as port-pin banking was not used to expand program memory beyond 64kB.

Finally, since the DS89C430/DS89C450 still support the standard 8051 multiplexed address bus scheme, external code and program memory can still be used in the application, if desired.

Serial Bootloader

While the DS8xC520 includes internal EPROM program memory, there is no provision for in-system or in-application programming (IAP) of the internal EPROM. A stand-alone programmer must be used to load the EPROM, and the DS8xC520 must be removed from (or electrically isolated from) the rest of the system for reprogramming to occur. (It is possible, however, to implement a user loader on the DS8xC520 which allows an external program or data EPROM or nonvolatile RAM to be reloaded under application control. See application note 102, "[Using the High-Speed Microcontroller as a Bootstrap Loader](#)," for more details.)

The DS89C430/DS89C450 improve on this programming process by including a serial bootloader function. This function allows program memory to be reloaded by using a simple ASCII-based protocol. The serial bootloader is implemented in the microcontroller's on-board ROM, so no code space is consumed by this feature. In addition, the FCNTL and FDATA registers can be used for IAP, so parts of the flash can be erased and rewritten under user control.

GPIO Port 0

Since the DS89C430/DS89C450 (like the DS8xC520) can operate without external code or data memory if desired, their eight Port 0 pins (which act as AD[7:0] when the multiplexed bus is active) can be used as general-purpose I/O (GPIOs). There are other I/O pins that can be reclaimed for general-purpose use when the external bus is not used: the eight Port 2 pins (P2[7:0]); the P3.6 (nWR) pins; and P3.7 (nRD) pins.

Unlike the Port 2 and Port 3 pins, however, the Port 0 pins use open-drain output drivers. This means that pullup resistors must be used, if these pins are to act as outputs. If the Port 0 pins will be used as inputs (driven externally), no pullup resistors are required.

Divide-by-1 Timer Clocks

The CKMOD register on the DS89C430/DS89C450 adds the ability to drive the three timers (Timer 0, Timer 1, and Timer 2) directly from the system clock (as opposed to the standard divide-by-4 and divide-by-12 options). This high-speed select mode (controlled by the bits T0MH, T1MH, and T2MH) defaults to disable following reset to make the timers compatible with code written for the DS80C310/DS80C320/DS80C323/DS8xC520.

Crystal Multiplier

The DS89C430/DS89C450 include an on-board crystal multiplier which allows the crystal frequency to be boosted by 2x or 4x. This means that a 5MHz crystal can be used to generate a 5MHz, 10MHz, or 20MHz clock as needed.

Five-Level Interrupt Priority

The DS89C430/DS89C450 expand the programmable interrupt priority scheme to allow any of the external interrupts, timer interrupts, serial port interrupts, or the watchdog interrupt to be assigned a user-defined priority level from 0 (lowest) to 3 (highest nonpower-fail priority). The highest priority level, level 4, is reserved for the power-fail interrupt. This system is backwards compatible with the low-/high-programmable priority scheme used by the DS80C310/DS80C320/DS80C323/DS8xC520.

Power-Supply Considerations

With their increased processing power, the DS89C430/DS89C450 have higher power-supply requirements than the microcontrollers in the high-speed family. At the maximum crystal frequency in active mode, the DS89C430/DS89C450 can draw up to 110mA (75mA, typ) in supply current. Consequently, when upgrading to the DS89C430/DS89C450, their power consumption may require changes to the power-supply circuit of a high-speed design. Refer to the device's data sheet for more details.

Digital Noise Considerations

The improved performance of the ultra-high-speed flash microcontrollers is the result of a core redesign that reduces machine cycle time and significantly increases internal switching speeds. Because of this, system designers can see a slight increase in digital noise when an ultra-high-speed flash microcontroller directly replaces a high-speed microcontroller. System designers should investigate what, if any, effect the increase in performance will have on their design. In some cases, it may be necessary to add additional bypass capacitors at the microcontroller or apply some other filtering method to reduce digital noise.

Software Timing Loops

Application code that generates precise timing using software loops may need to be adjusted when moving from the high-speed microcontrollers to the ultra-high-speed devices. Timing loops of this type must be examined on a case-by-case basis, however, since not all instructions show the maximum 4x speed improvement when moving to the DS89C430/DS89C450. For example, while "ADD A, R0" executes in 4 clock cycles on any of the high-speed microcontrollers and in 1 clock cycle on the DS89C430/DS89C450 (a 4x speed increase), the instruction "ADD A, @R0" goes from 4 cycles on the high-speed devices to 2 cycles on the DS89C430/DS89C450 (a 2x speed increase). Refer to the "Instruction Timing" sections in both the *High-Speed Microcontroller User's Guide* and the *Ultra-High-Speed Flash Microcontroller User's Guide* for more details.

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